

Round Rock MLK 13.3" Schematics Document

Broadwell ULT

2015-08-19

REV : A00

DY : None Installed

XDP: For CPU XDP Debug Port installed

PCH_XDP: For PCH XDP Debug Port installed

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Cover Page

Size
A3

Document Number

Round Rock MLK 13.3"

Rev
A00

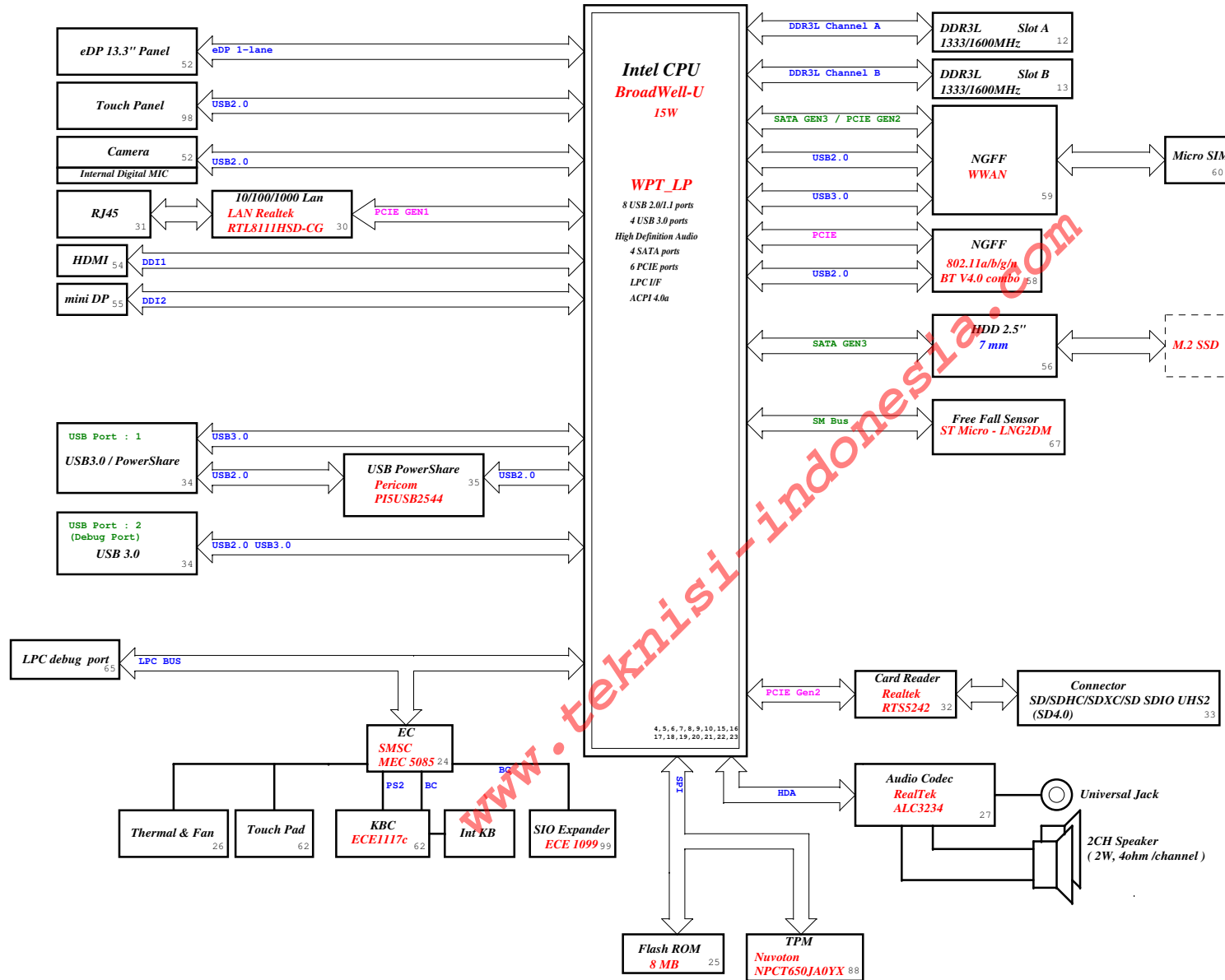
Date: Wednesday, August 19, 2015

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Round Rock MLK 13.3" Block Diagram

Project code : 4PD06F010001
PCB P/N : 15203
Revision : A00


CHARGER	
BQ24777	44
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC	
TPS51275	45
INPUTS	OUTPUTS
DCRATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5
CPU DC/DC	
TPS51624	46-47
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE
SYSTEM DC/DC	
SY8206DQNC	48
INPUTS	OUTPUTS
DCRATOUT	1D05V_M
SYSTEM DC/DC	
SY8206DQNC & APL5338	49
INPUTS	OUTPUTS
DCRATOUT	1D35V_S3 0D675V_SB DDR_VREF_S3
Load Switches	
36	
INPUTS	OUTPUTS
5V_S3 3D3V_S3	5V_S0 3D3V_S0 3D3V_S5_PCH 3D3V_M 3D3V_LAN 1D05V_MODPHY 1D05V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top	L6:Bottom
L2:PWR/GND	
L3:Signal	
L4:Signal	
L5:PWR/GND	



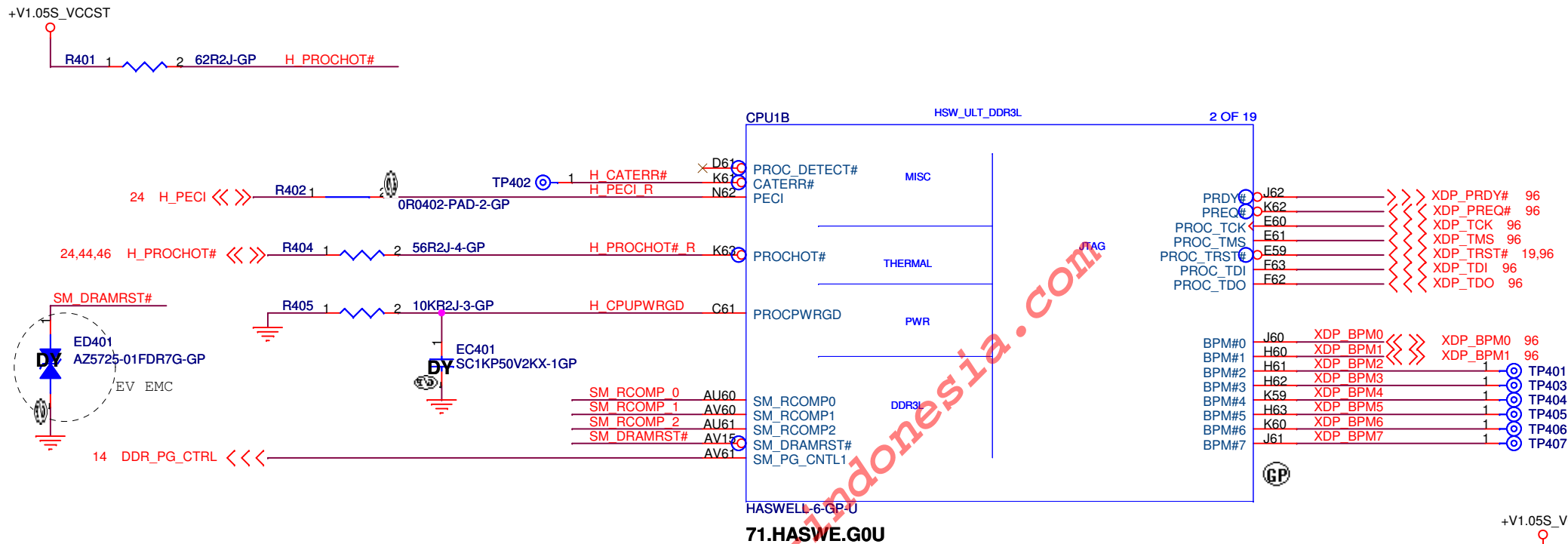
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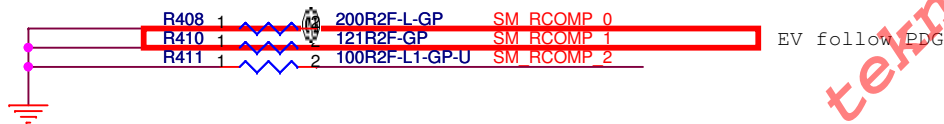
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (PCIE/DMI/FDI)			
Size A4	Document Number		Rev A00
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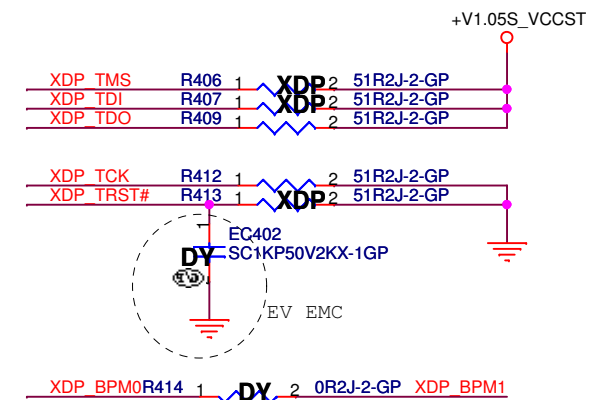
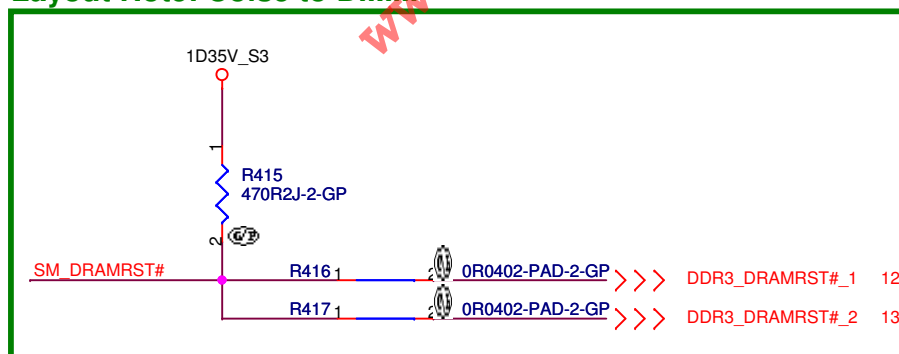
SSID = CPU



Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



Layout Note: Colse to DIMM



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Title **CPU (THERMAL/CLOCK/PM)**

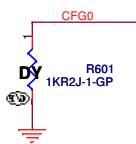
Size A4 Document Number **Round Rock MLK 13.3"** Rev **A00**

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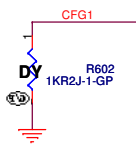


SSID = CPU

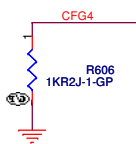
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0: Lane Reversed 1: (Default) Normal Operation; No stall



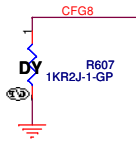
PCH/PCH LESS MODE SELECTION	
CFG1	0: Lane Reversed 1: (Default) Normal Operation



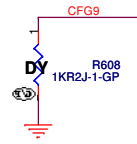
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



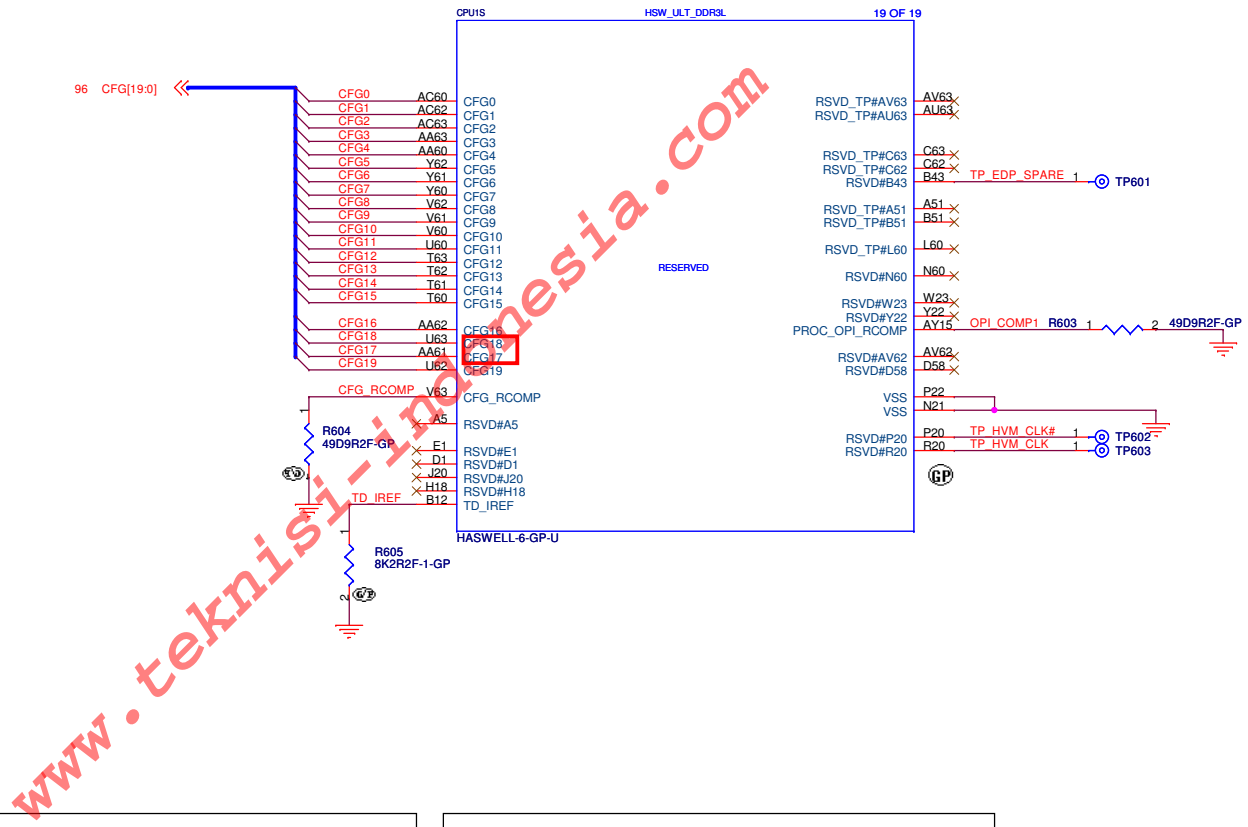
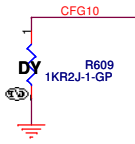
ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegrardless of the locking of the unit



NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0: No VR support SVID is present The chip will not generate(OR Respond to) SVID activity



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



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Title: **CPU (XDP)**

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Round Rock MLK 13.3"		

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Layout Note: R702 should be placed within 2 inches (50.8 mm) of the processor.

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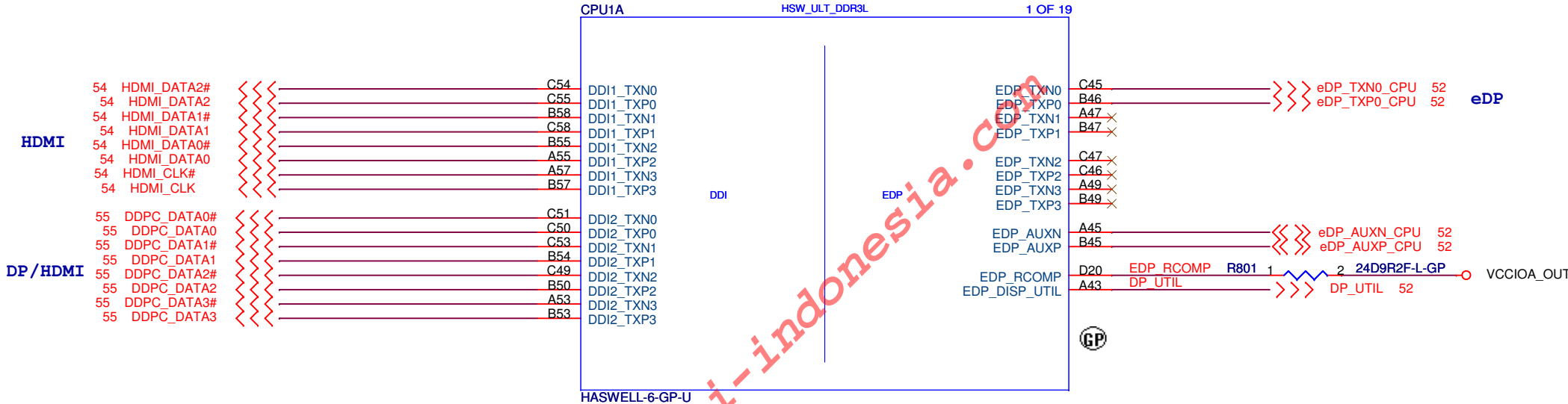
46 VR_SVID_ALERT#
46 H_CPU_SVIDCLK
46 H_CPU_SVIDDAT
36,96 H_VCCST_PWRGD
36,46 H_VR_ENABLE
36 H_VR_READY

```

[illegible]


Title			
<i>CPU (VCC_CORE)</i>			
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Custom		<i>Round Rock MLK 13.3"</i>	<i>A00</i>
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SSID = CPU



DDI	HDMI	Display Port
DDI_TXN0	HDMI_DATA2_N	DP_LANE0_N
DDI_TXP0	HDMI_DATA2_P	DP_LANE0_P
DDI_TXN1	HDMI_DATA1_N	DP_LANE1_N
DDI_TXP1	HDMI_DATA1_P	DP_LANE1_P
DDI_TXN2	HDMI_DATA0_N	DP_LANE2_N
DDI_TXP2	HDMI_DATA0_P	DP_LANE2_P
DDI_TXN3	HDMI_CLK_N	DP_LANE3_N
DDI_TXP3	HDMI_CLK_P	DP_LANE3_P

<Core Design>



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Title

CPU (DDI/EDP)

SizeA4

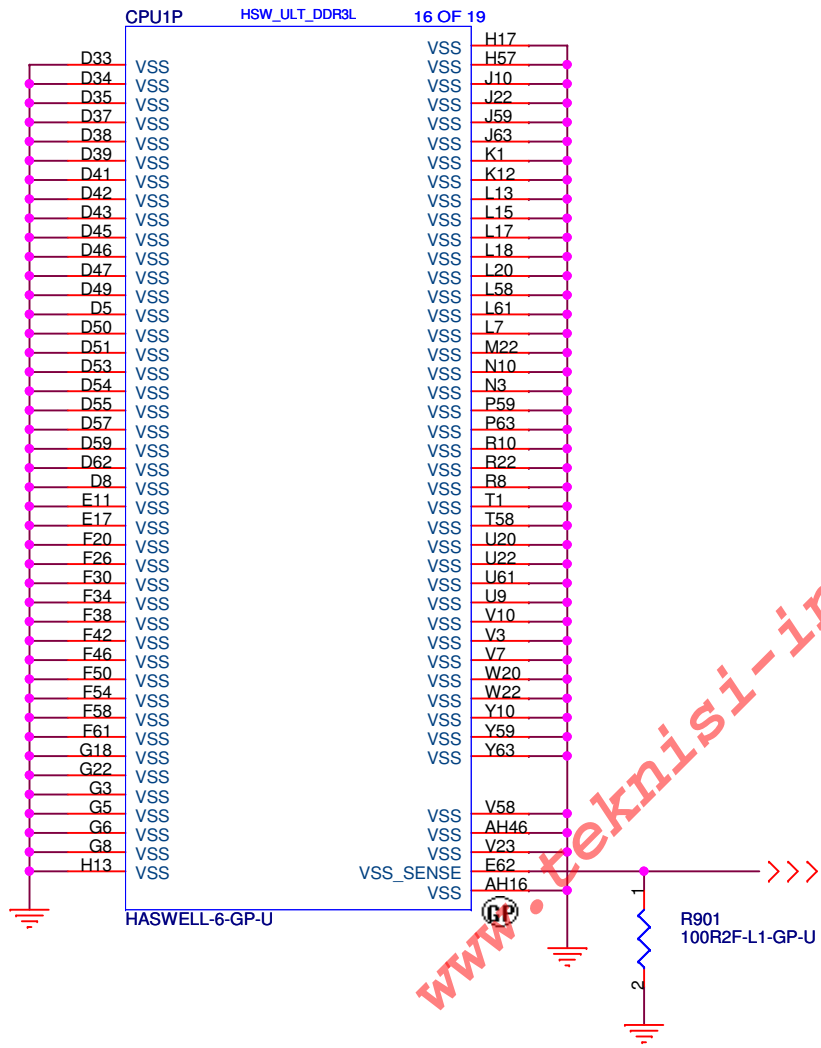
Document Number

RevA00

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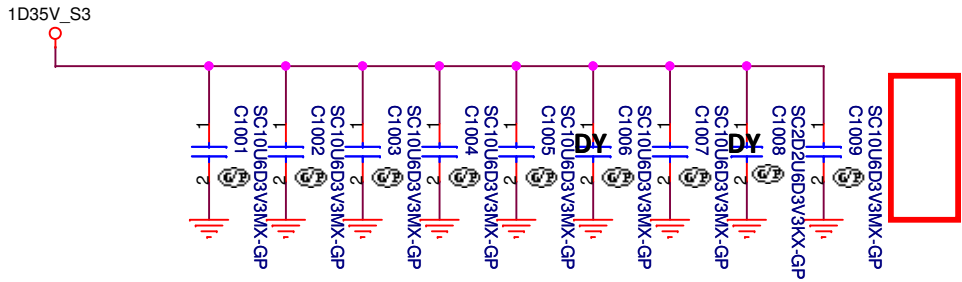
SSID = CPU



Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals


<Core Design>

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Title			
CPU (VSS)			
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Title			
CPU (Power CAP1)			
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Title

CPU (Power CAP2)

Size
A

Document Number

Round Rock MLK 13.3"

Rev

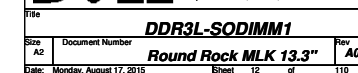
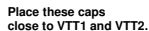
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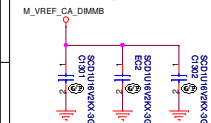
SSID = MEMORY

Place these caps close to VREF_CA



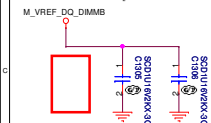
Layout Note:

Place these caps close to VREF_CA

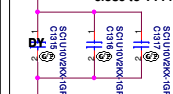


Layout Note:

Place these caps close to VREF_DQ



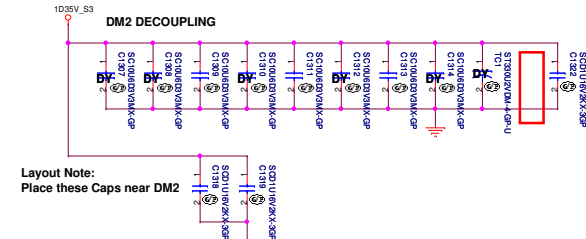
Place these caps close to VTT1 and VTT2.



DQS1	DQ0	M_B_DQ8
	DQ1	M_B_DQ14
	DQ2	M_B_DQ10
	DQ3	M_B_DQ11
	DQ4	M_B_DQ12
	DQ5	M_B_DQ9
	DQ6	M_B_DQ13
DQS3	DQ8	M_B_DQ28
	DQ9	M_B_DQ29
	DQ10	M_B_DQ26
	DQ11	M_B_DQ27
	DQ12	M_B_DQ25
	DQ13	M_B_DQ24
	DQ14	M_B_DQ30
DQS5	DQ16	M_A_DQ40
	DQ17	M_A_DQ41
	DQ18	M_A_DQ46
	DQ19	M_A_DQ42
	DQ20	M_A_DQ45
	DQ21	M_A_DQ44
	DQ22	M_A_DQ47
DQS7	DQ24	M_A_DQ56
	DQ25	M_A_DQ57
	DQ26	M_A_DQ59
	DQ27	M_A_DQ58
	DQ28	M_A_DQ61
	DQ29	M_A_DQ60
	DQ30	M_A_DQ63
DQS0	DQ32	M_A_DQ4
	DQ33	M_A_DQ1
	DQ34	M_A_DQ3
	DQ35	M_A_DQ7
	DQ36	M_A_DQ5
	DQ37	M_A_DQ0
	DQ38	M_A_DQ2
DQS2	DQ40	M_A_DQ21
	DQ41	M_A_DQ20
	DQ42	M_A_DQ22
	DQ43	M_A_DQ23
	DQ44	M_A_DQ16
	DQ45	M_A_DQ17
	DQ46	M_A_DQ19
DQS4	DQ48	M_A_DQ36
	DQ49	M_A_DQ33
	DQ50	M_A_DQ35
	DQ51	M_A_DQ39
	DQ52	M_A_DQ37
	DQ53	M_A_DQ32
	DQ54	M_A_DQ34
DQS6	DQ56	M_A_DQ52
	DQ57	M_A_DQ49
	DQ58	M_A_DQ48
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	DQ60	M_A_DQ51
	DQ61	M_A_DQ55
	DQ62	M_A_DQ54



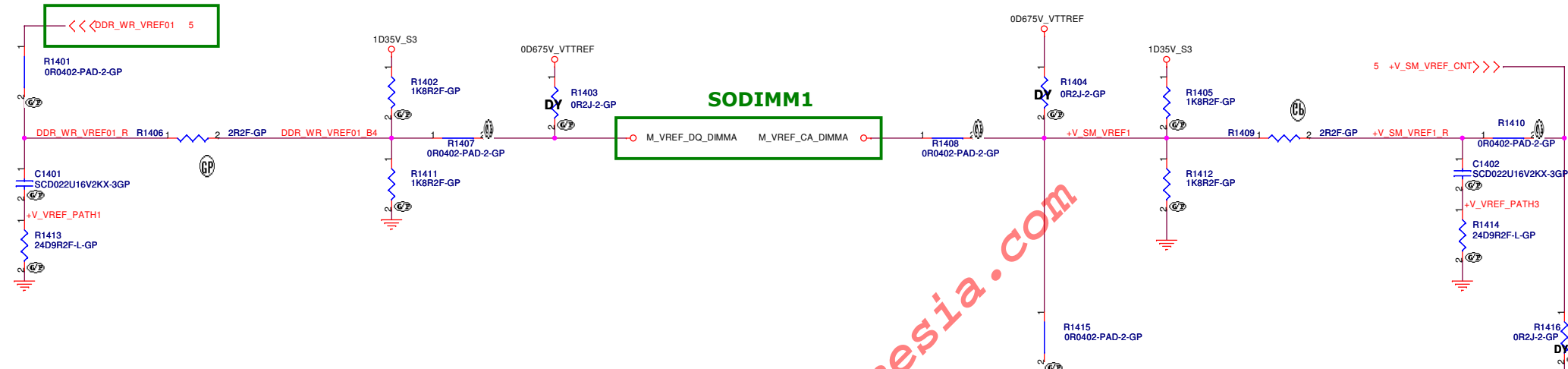
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA



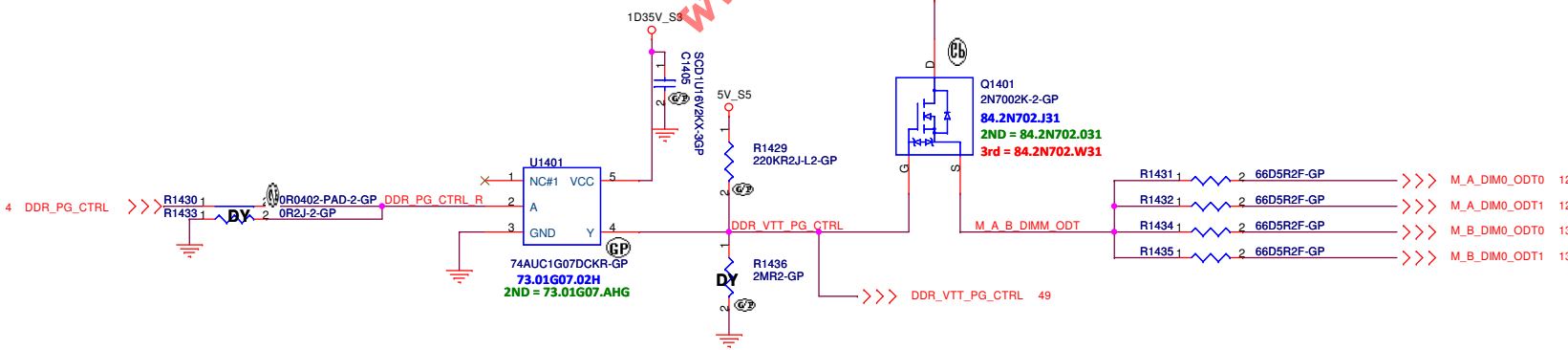
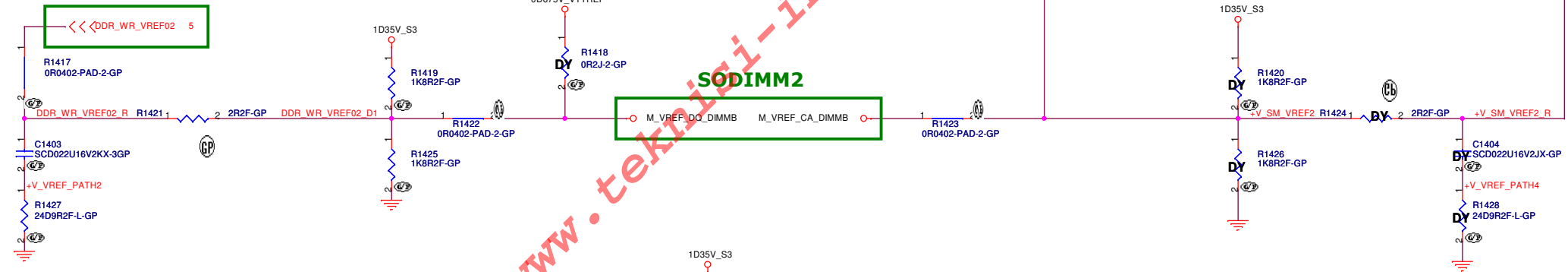
Layout Note:
Place these Caps near DM2

SSID = MEMORY VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

SA_DIMM_VREFDQ
Driven by process (PIN#AR51)



SB_DIMM_VREFDQ
Driven by process (PIN#AP51)



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Title: **M1 & M3 Implementation**

Size: A3	Document Number: Round Rock MLK 13.3"	Rev: A00
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SSID = PCH

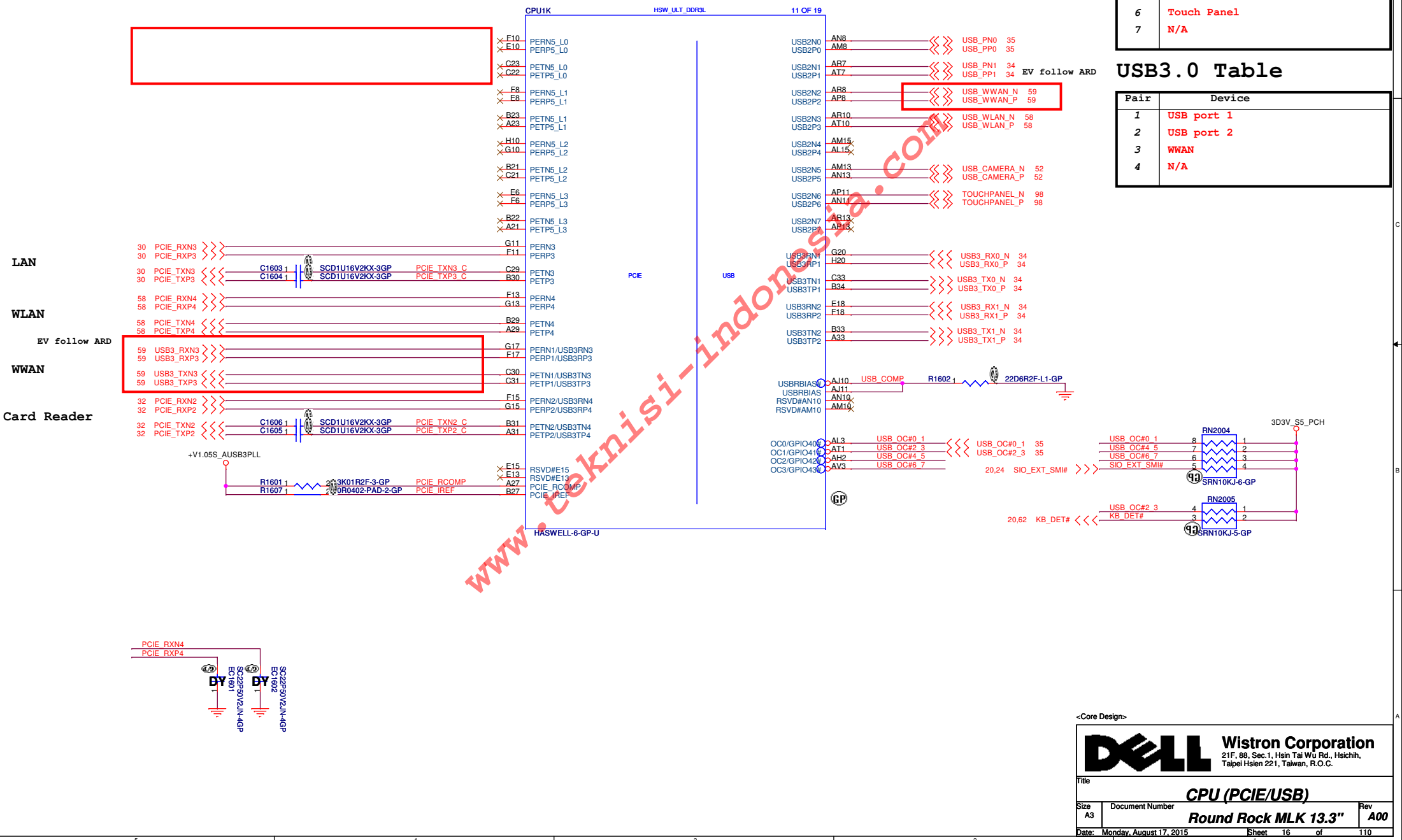
USB2.0 Table

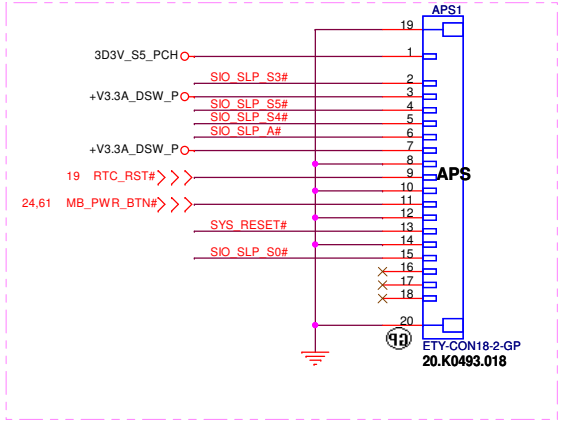
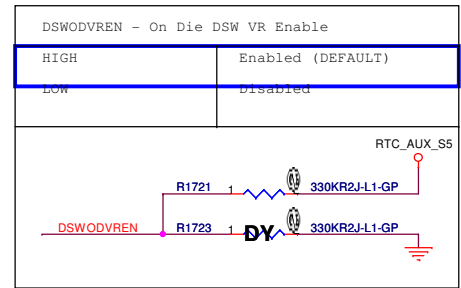
Pair	Device
0	USB port 1 (USB Charger)
1	USB port 2 (Win Debug)
2	WWAN
3	WLAN (BT)
4	N/A
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 Table

Pair	Device
1	USB port 1
2	USB port 2
3	WWAN
4	N/A

Broadwell ULT: ---
USB Ext. port 1
External debug port use on Broadwell ULT

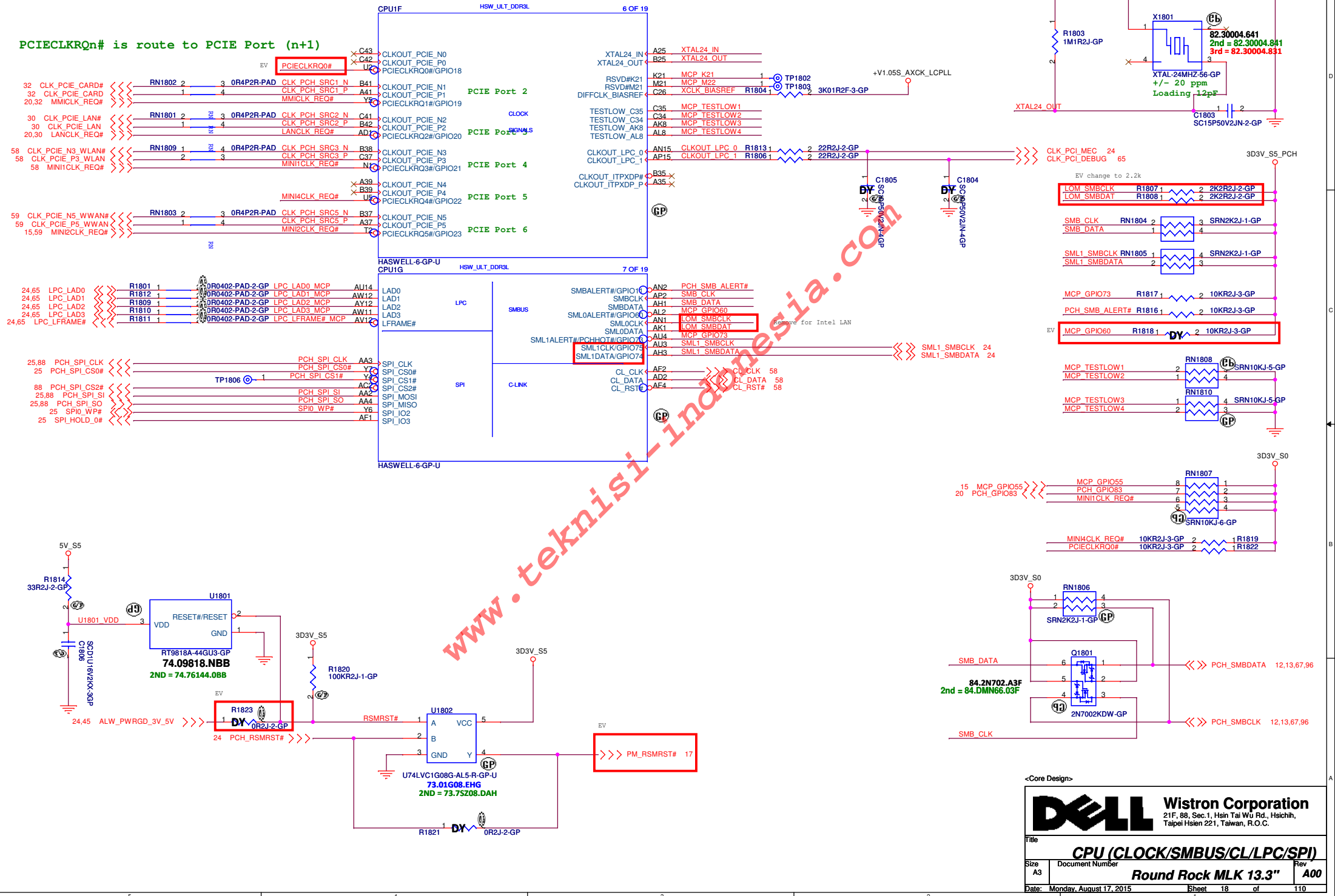


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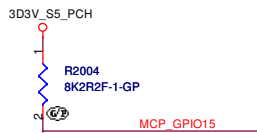
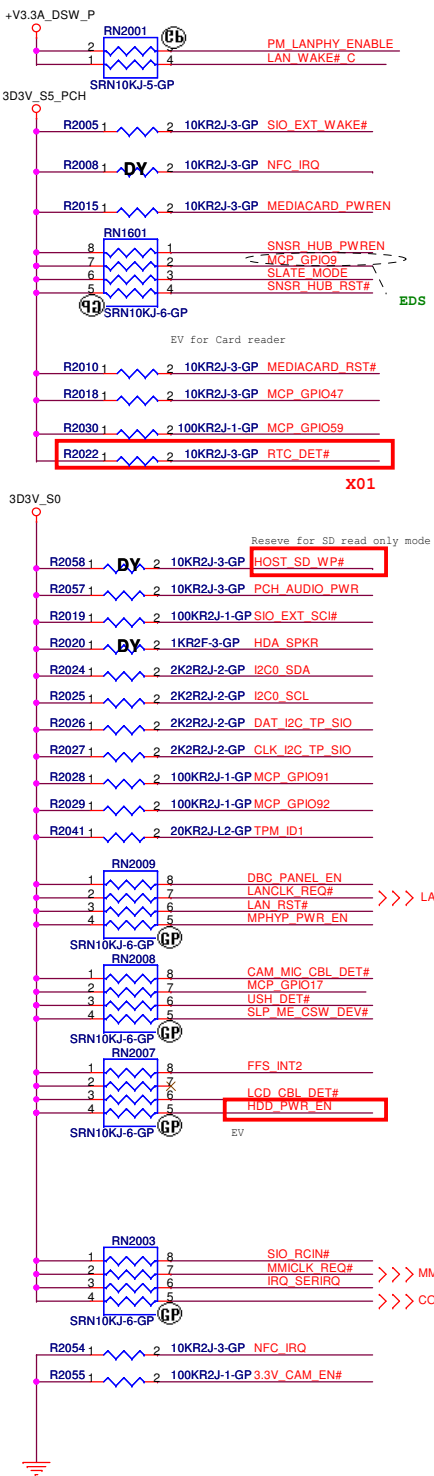
SSID = PCH

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PCIECLKRQn# is route to PCIE Port (n+1)

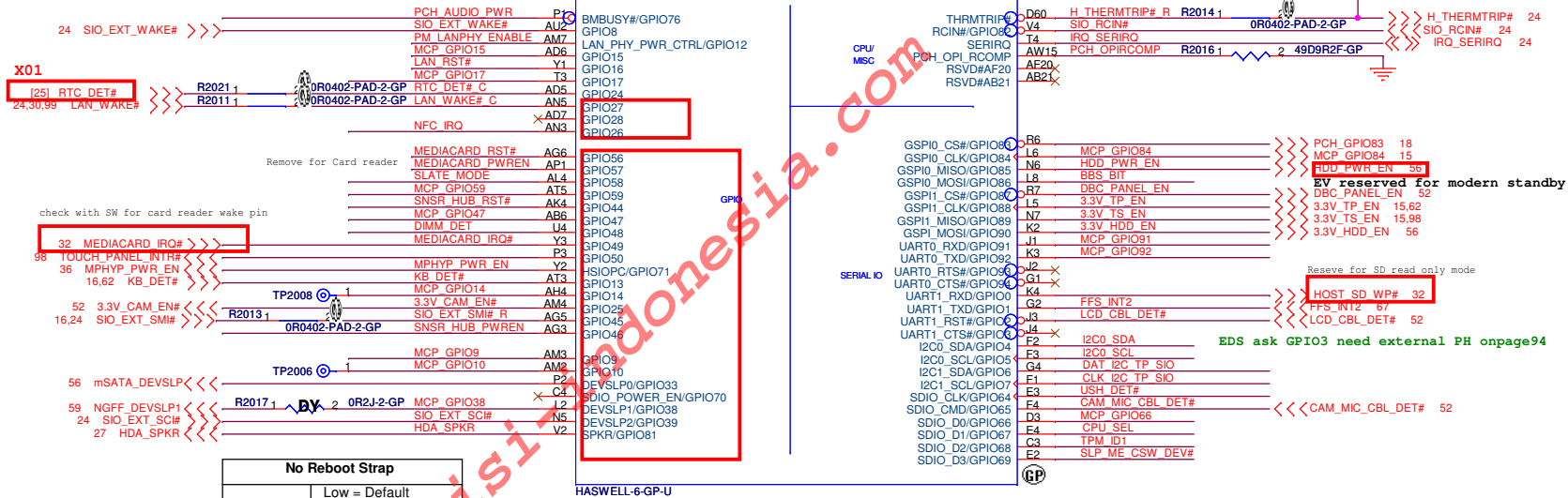


SSID = PCH

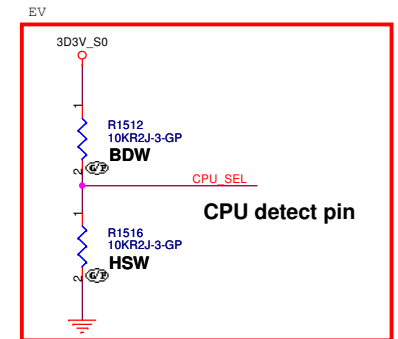
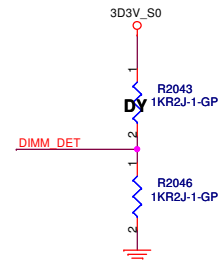
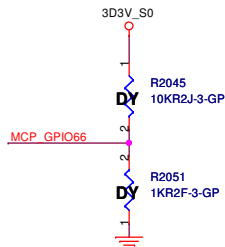
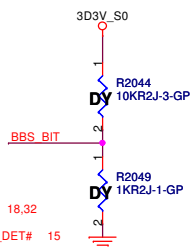


TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

EDS no ask GPIO9 required external PH



No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot



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Title

Size
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Document Number

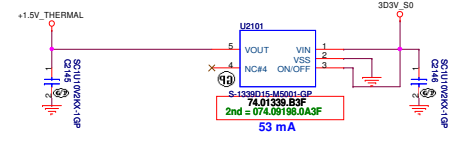
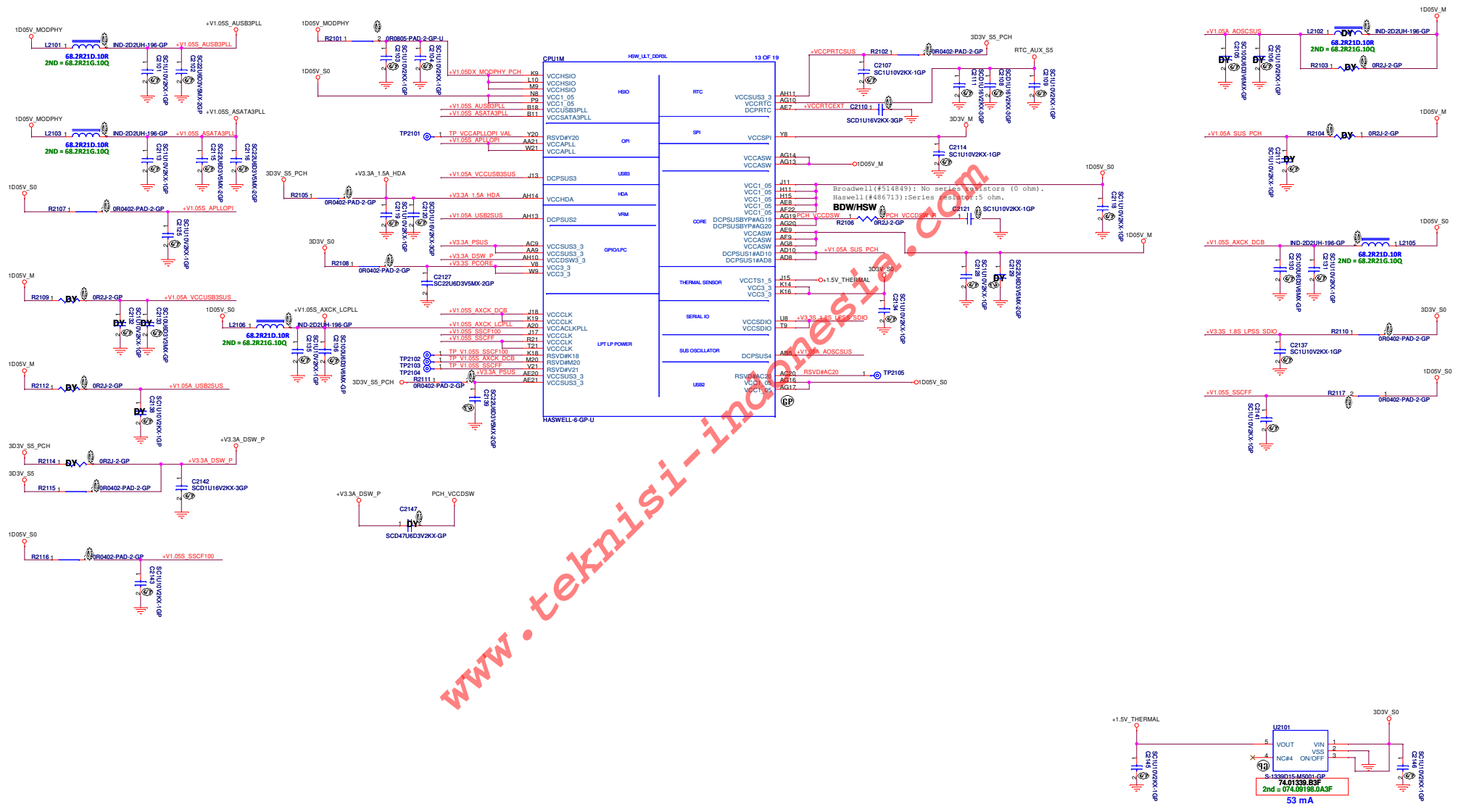
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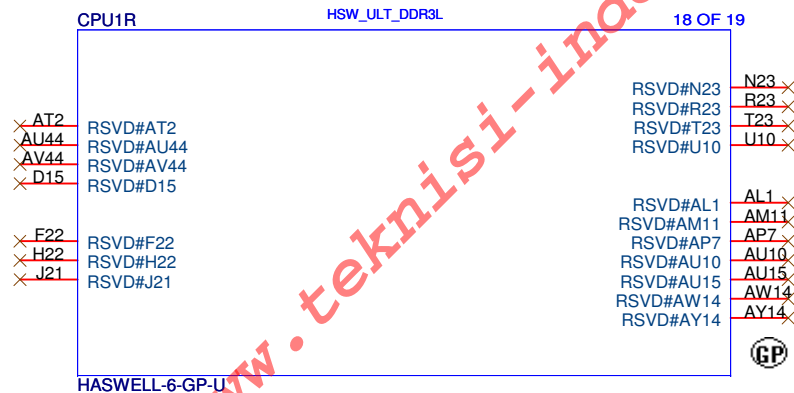
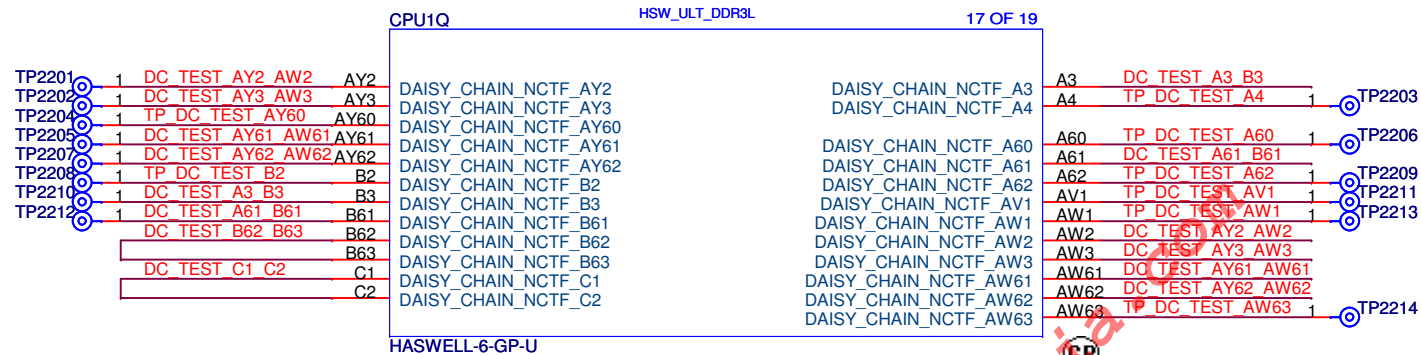
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CPU (GPIO/CPU)

Round Rock MLK 13.3"

Rev
A00





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Title

CPU (RSVD)

Size
A4

Document Number

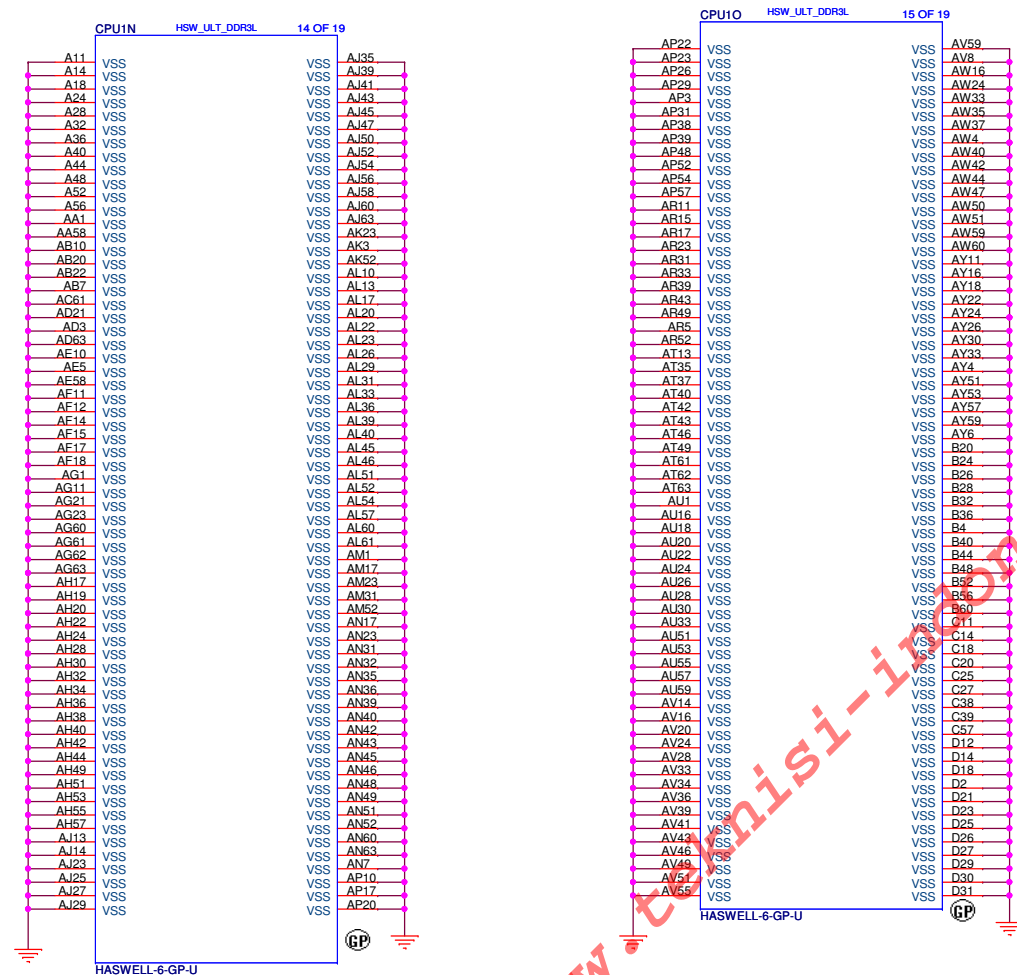
Round Rock MLK 13.3"

Rev
A00

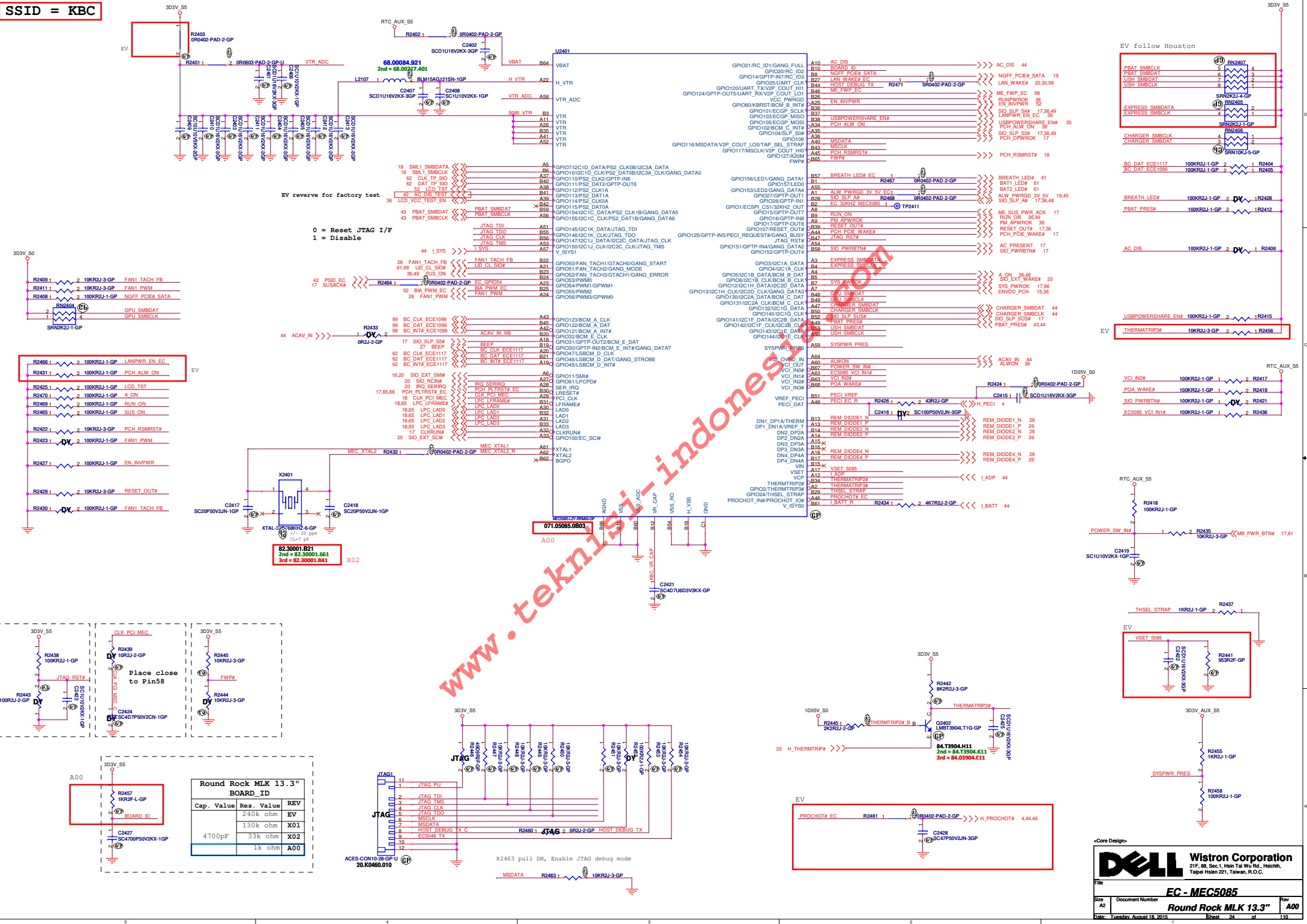
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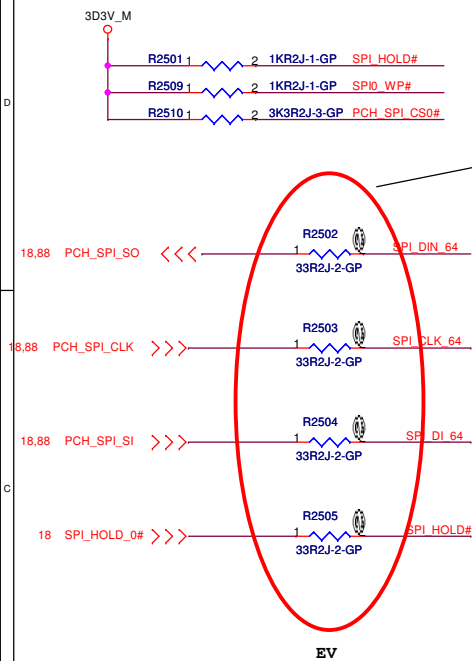
SSID = PCH



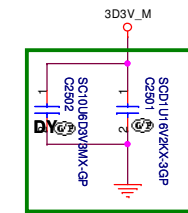
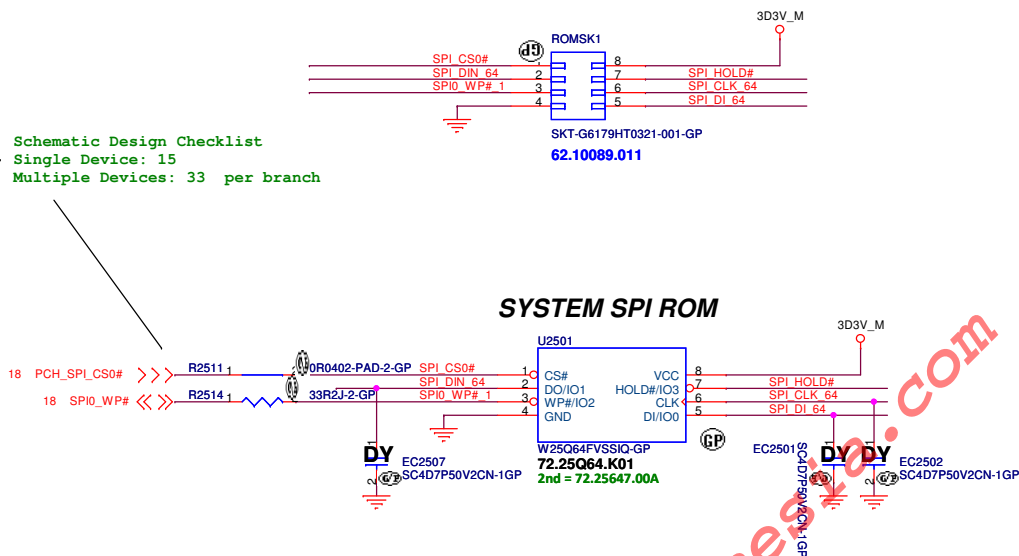
SSID = KBC



SPI ROM Equal length need to less than 500mil

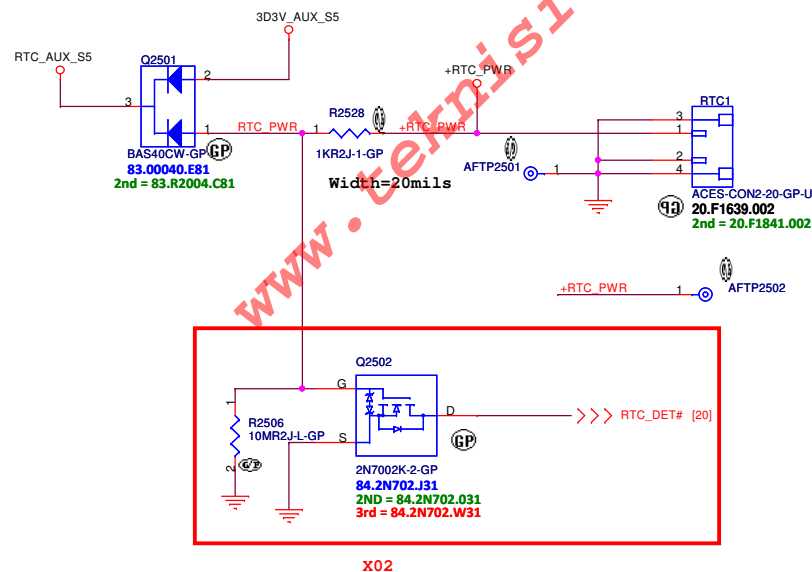


Schematic Design Checklist
Single Device: 15
Multiple Devices: 33 per branch



Layout Note: Close to U2501 Pin 8

SSID = RTC



<Variant Name>



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Title

Flash/RTC

Size
A3

Document Number

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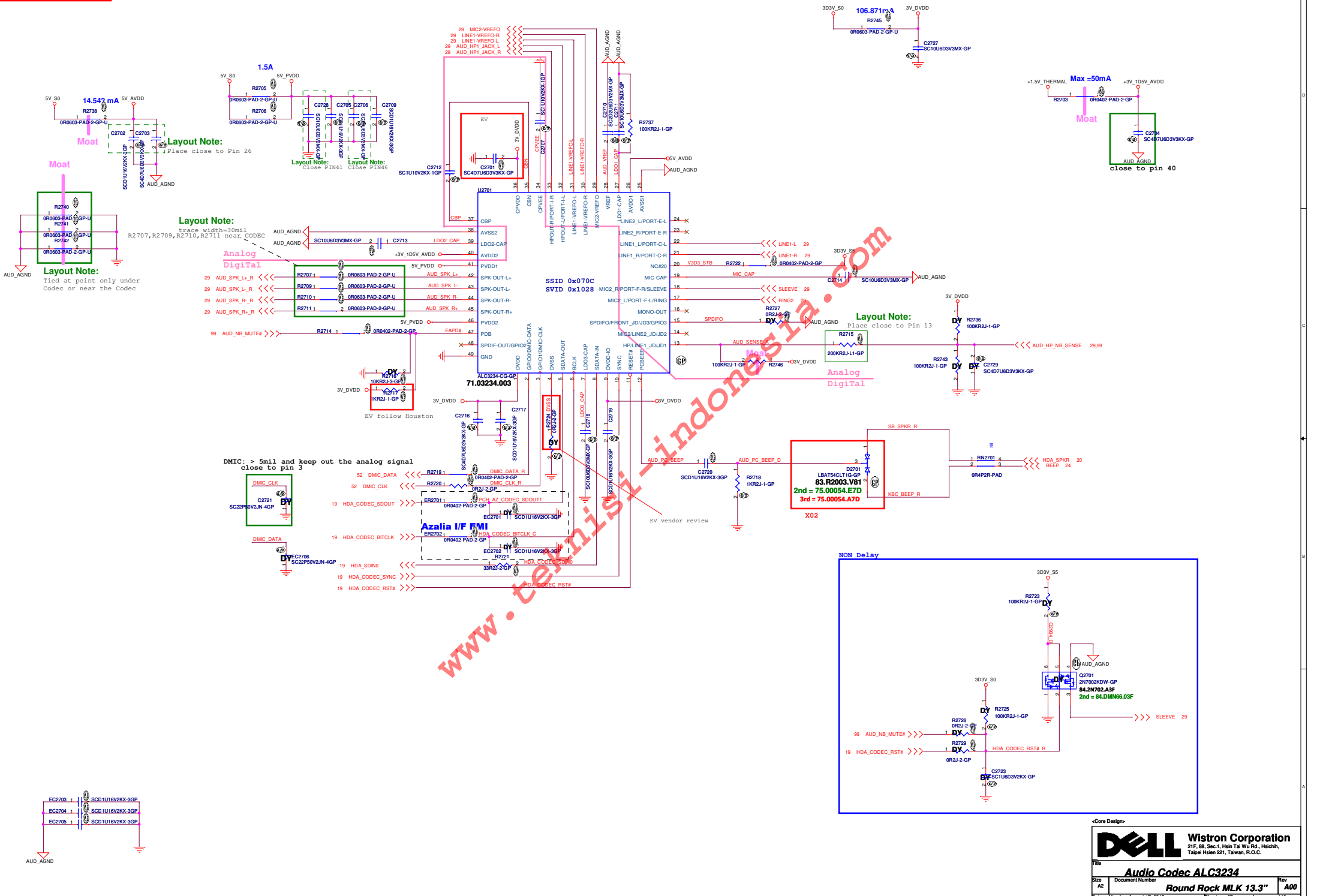
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<Core Design>

**Thermal/Fan**Rev
A0

Round Rock MLK 13.3"

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Title

Reserved

Size
A

Document Number

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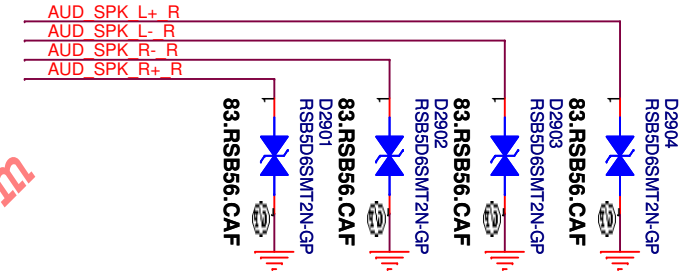
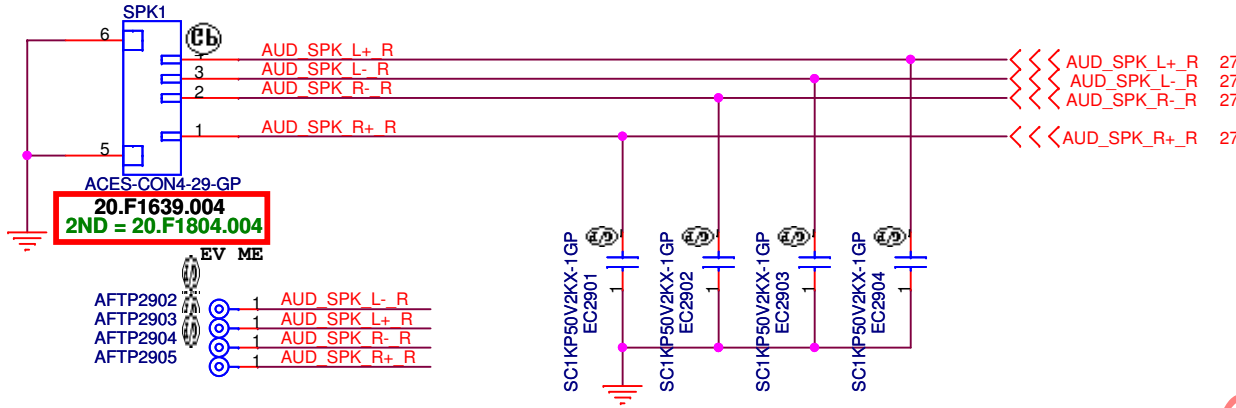
Rev
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Date: Monday, August 17, 2015

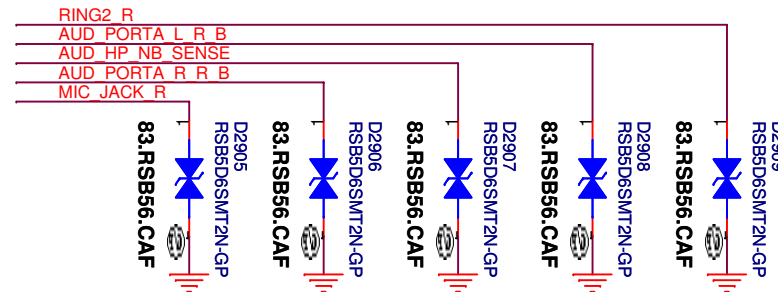
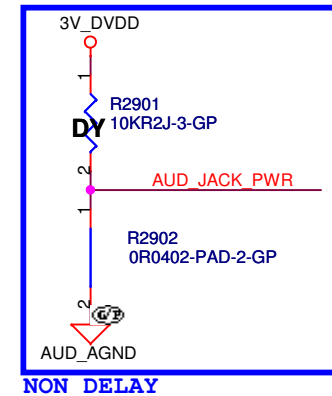
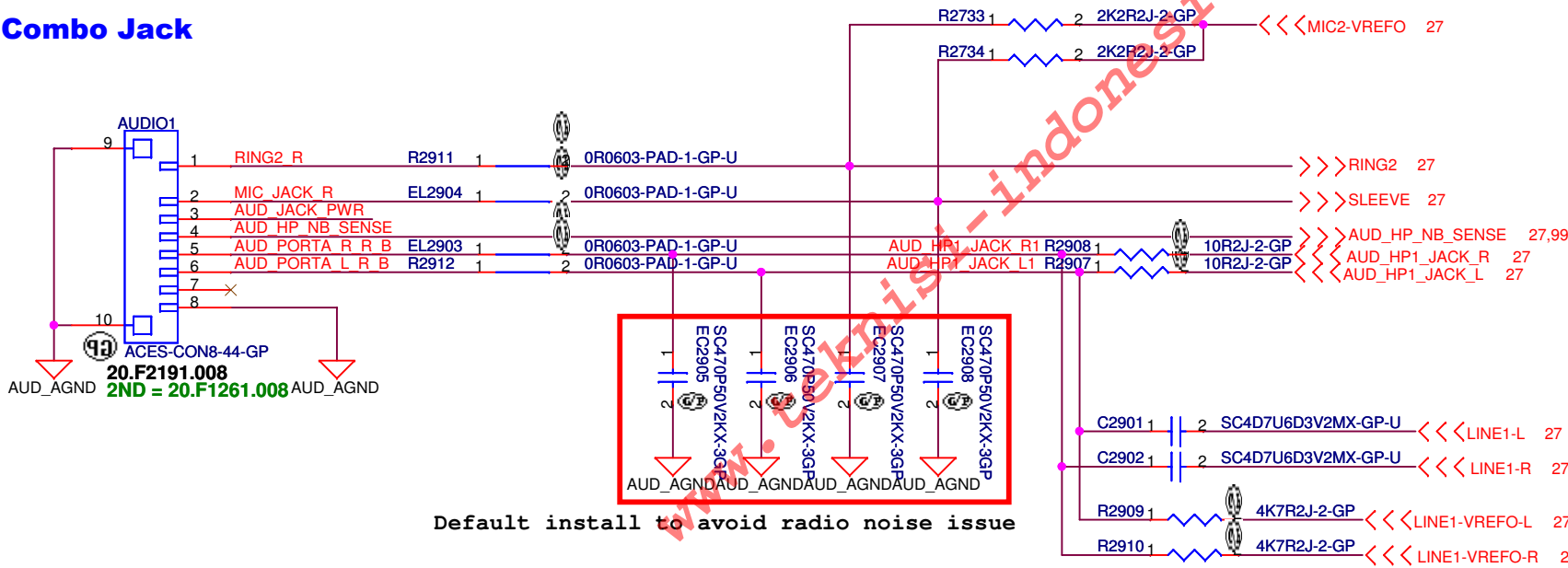
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SSID = AUDIO

Speaker 2W/ch



Combo Jack



<Core Design>



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Title

Speaker/HPMIC CONN

Size

Document Number

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A00

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LANXOUT

C3011

SC15P50V2JN-2-GP

X3001
XTAL-25MHZ-181-GP

82.30020.G71
2nd = 82.30020.D41

C3001

LANXIN

SC15P50V2JN-2-GP

3D3V_LAN rise time must be controlled between 0.5 mS and 100 mS.

3D3V_LAN

C3004

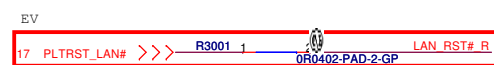
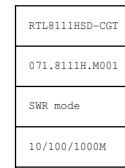
C3005

C3007

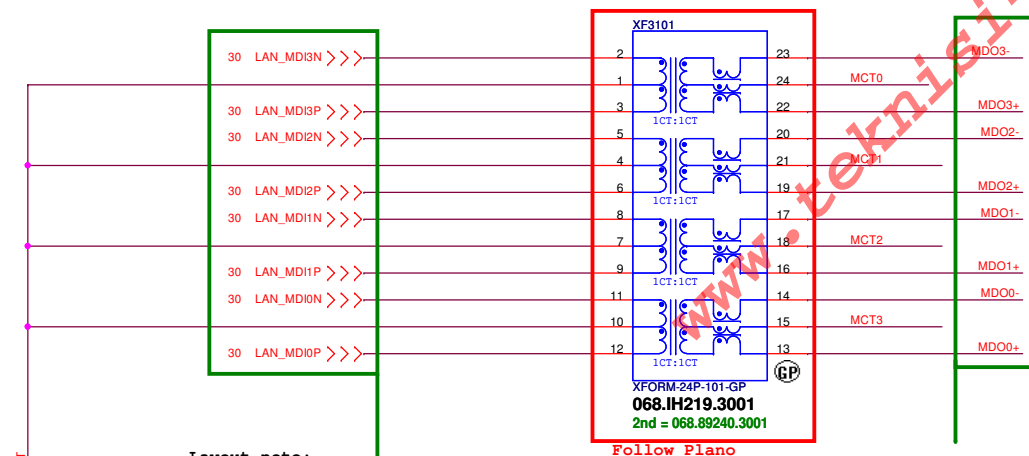
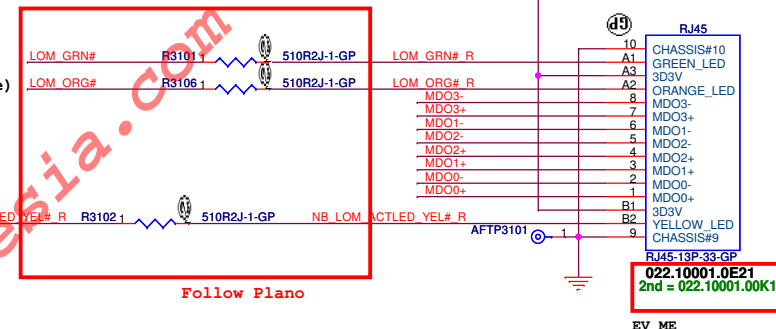
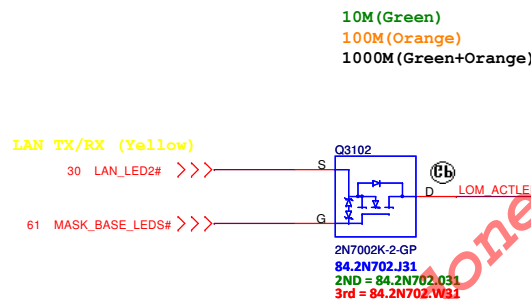
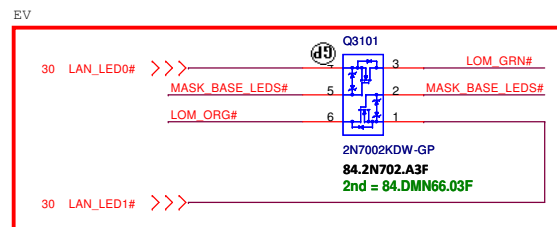
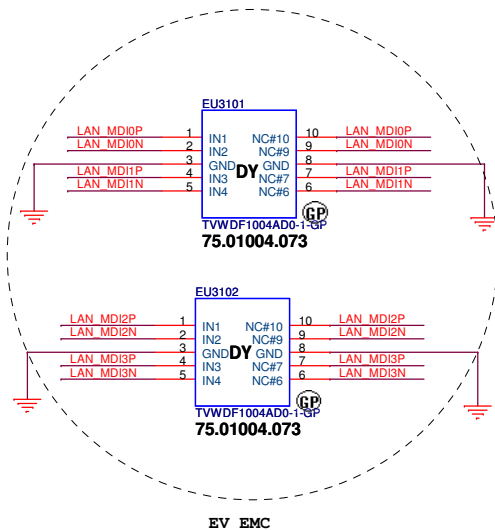
SC4D7J6D3V3KX-GP

SC4D7J6D3V3KX-GP

La
C3
C3

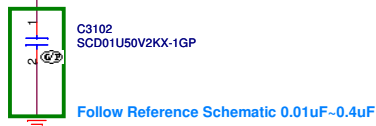
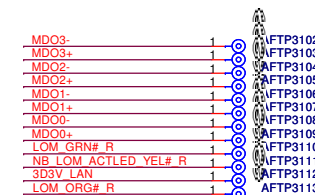
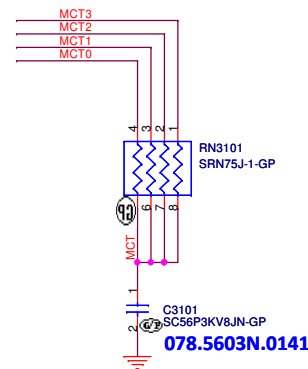


SSID = LOM



Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.



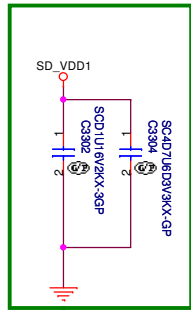
<Core Design>



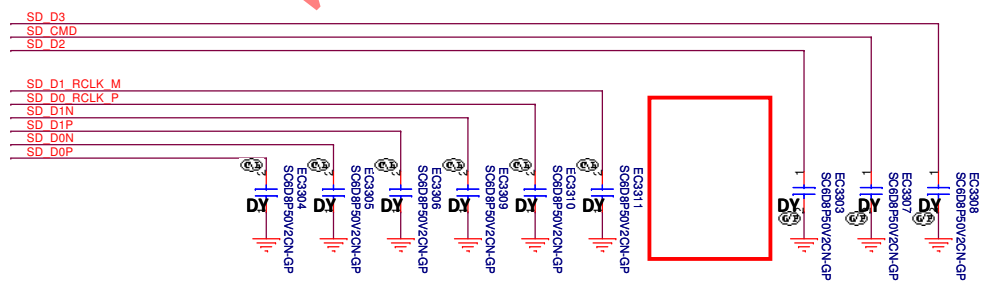
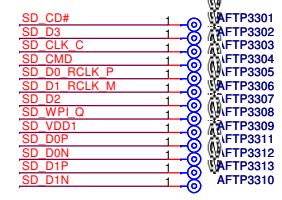
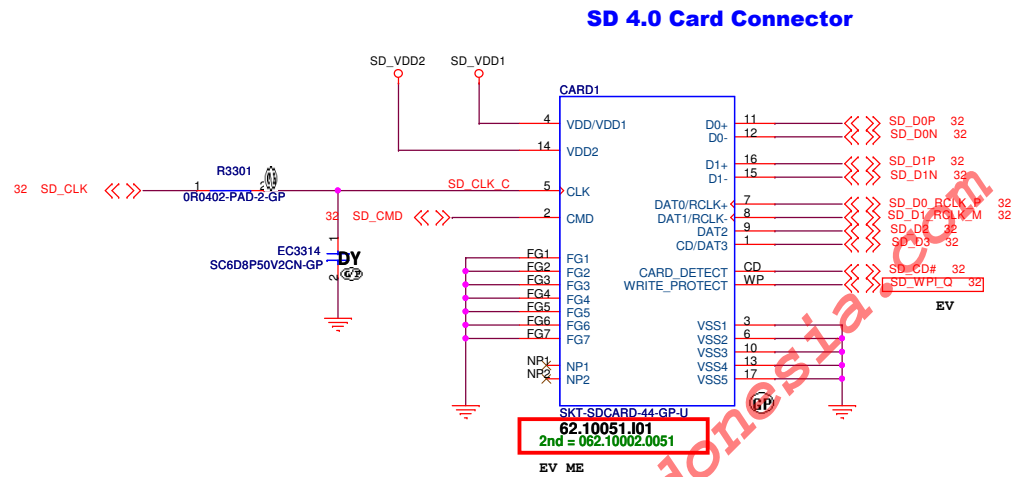
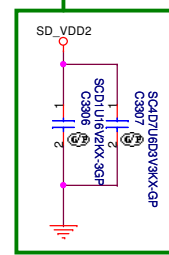
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Title		RJ45/Transformer	
Size	Document Number	Rev	
A3			
Date: Monday, August 17, 2015		Sheet	31 of 110
		Round Rock MLK 13.3A00	

SSID =Card Reader



Layout Note:Close to Card Reader CONN

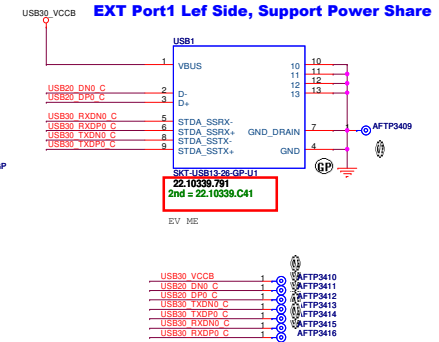
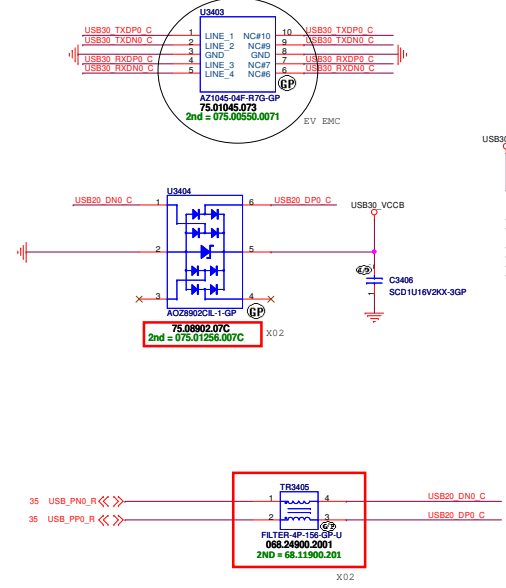
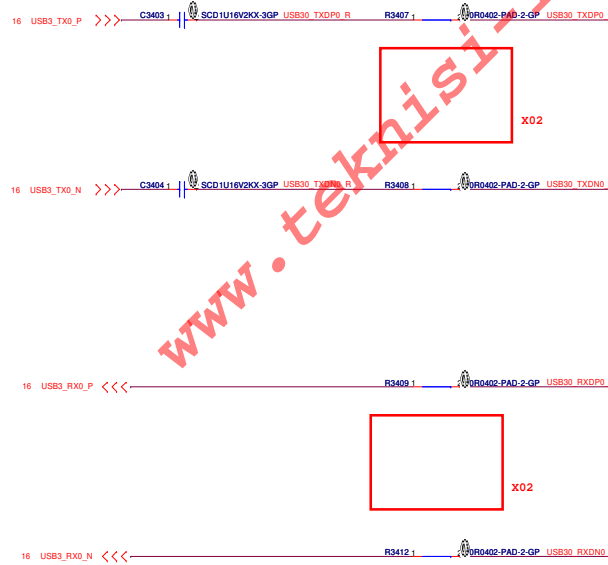
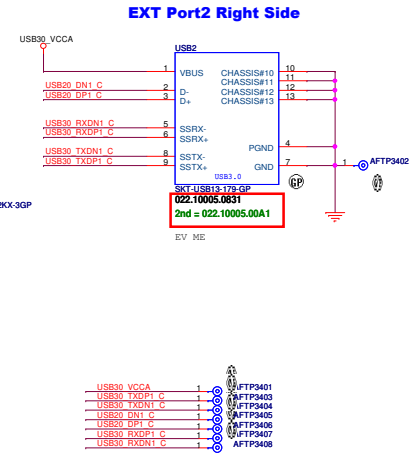
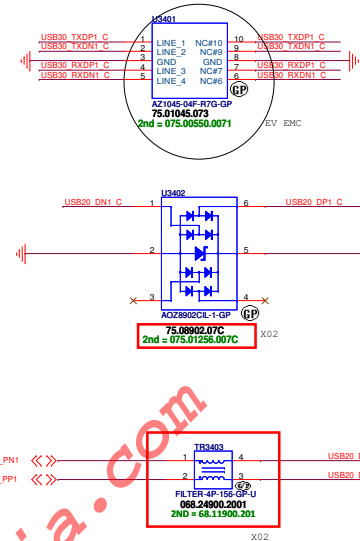


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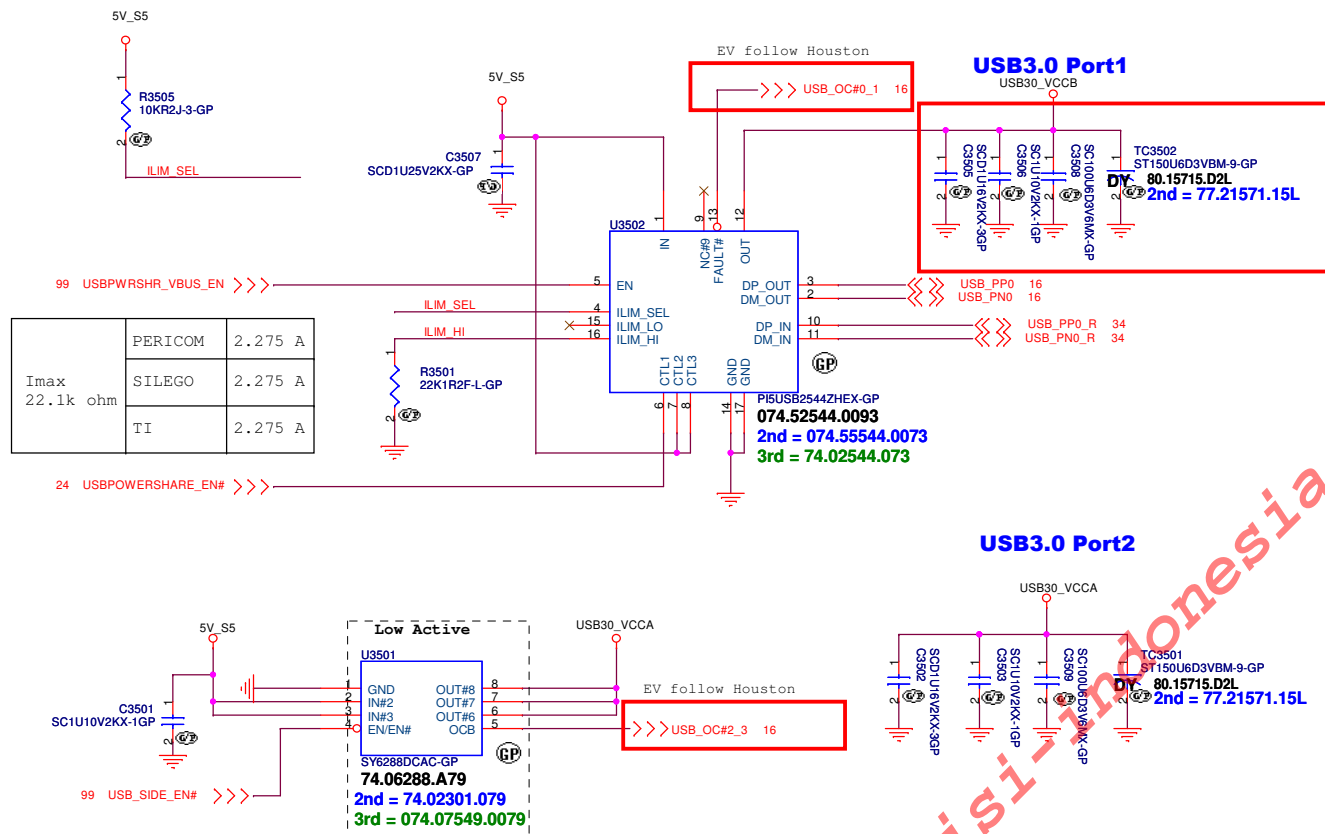
DELL Wistron Corporation
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Title **Card Reader CONN**

Size A3	Document Number Round Rock MLK 13.3"	Rev A00
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SSID = USB



PI5USB2544 Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	x	1	x	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	0	0	SDP1	ILIM_LO	Data lines connected
0	1	0	1	SDP1	ILIM_HI	
0	1	1	0	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data lines disconnected
1	0	0	0	DCP_Shorted	ILIM_LO	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	
1	0	1	0	Divider-1A	ILIM_LO	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data lines connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data lines connected


Note:
(1) No OUT discharge when changing between 1111 and 1110.

SSID = Reset.Suspend

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(Reserved)			
Size A4	Document Number		Rev A00
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<Variant Name>



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Size
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SSID = OBF'F

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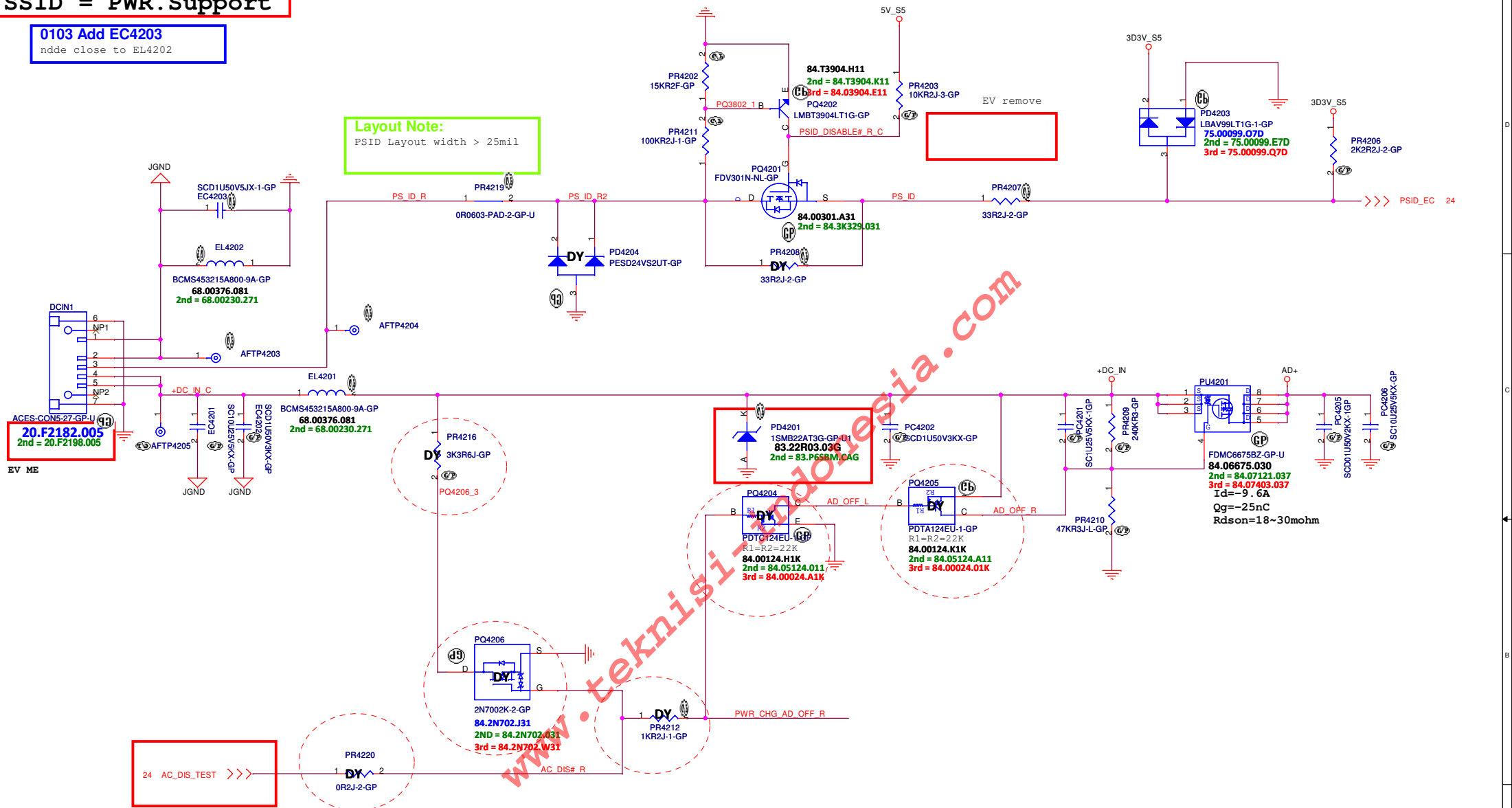
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Title Reserved			
Size A	Document Number Round Rock MLK 13.3"		Rev A00
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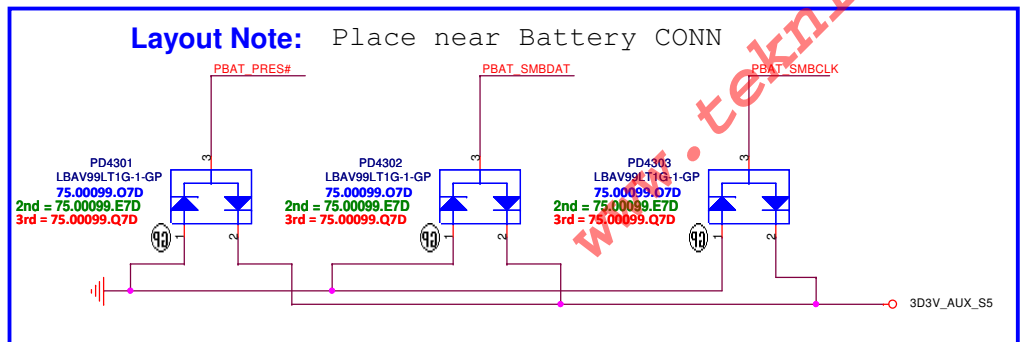
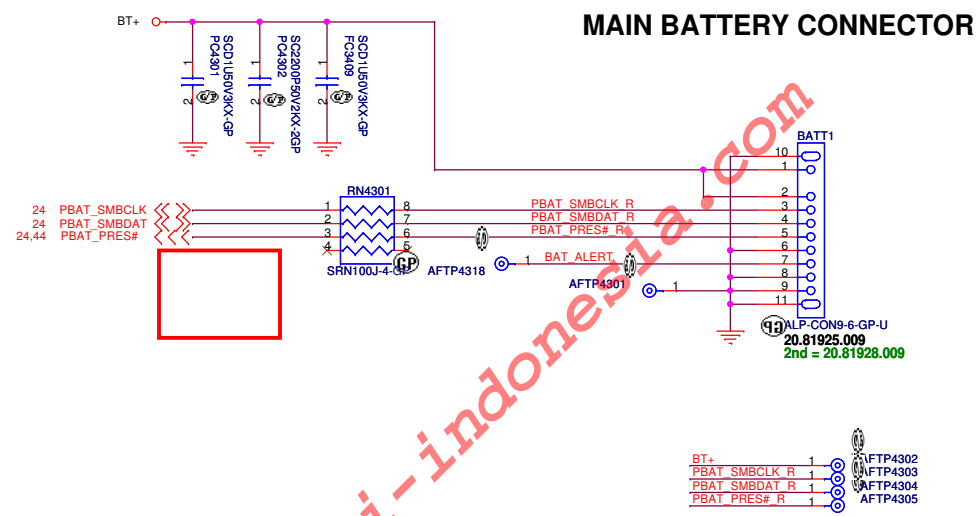
SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

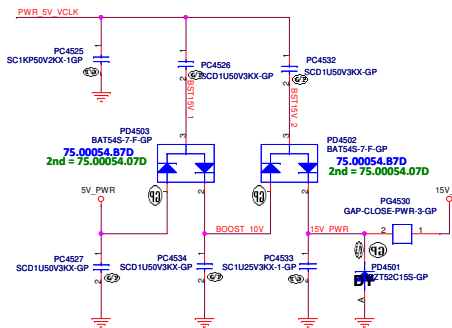
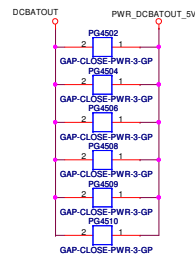
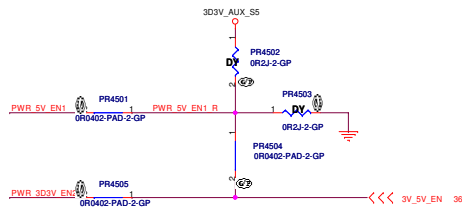
Layout Note:
PSID Layout width > 25mil



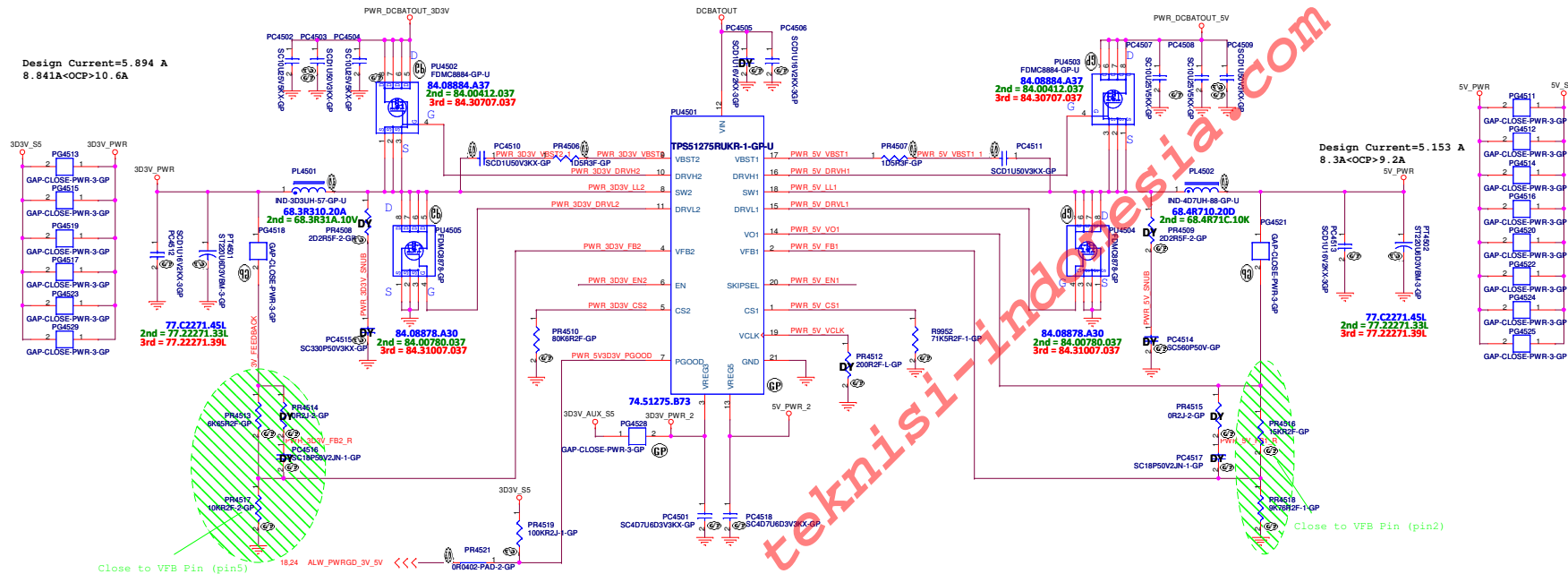
EV reverse for factory test, confirmed with SW there's no need to install




```
SSID = PWR.Plane.Regulator_5v3p3v
```



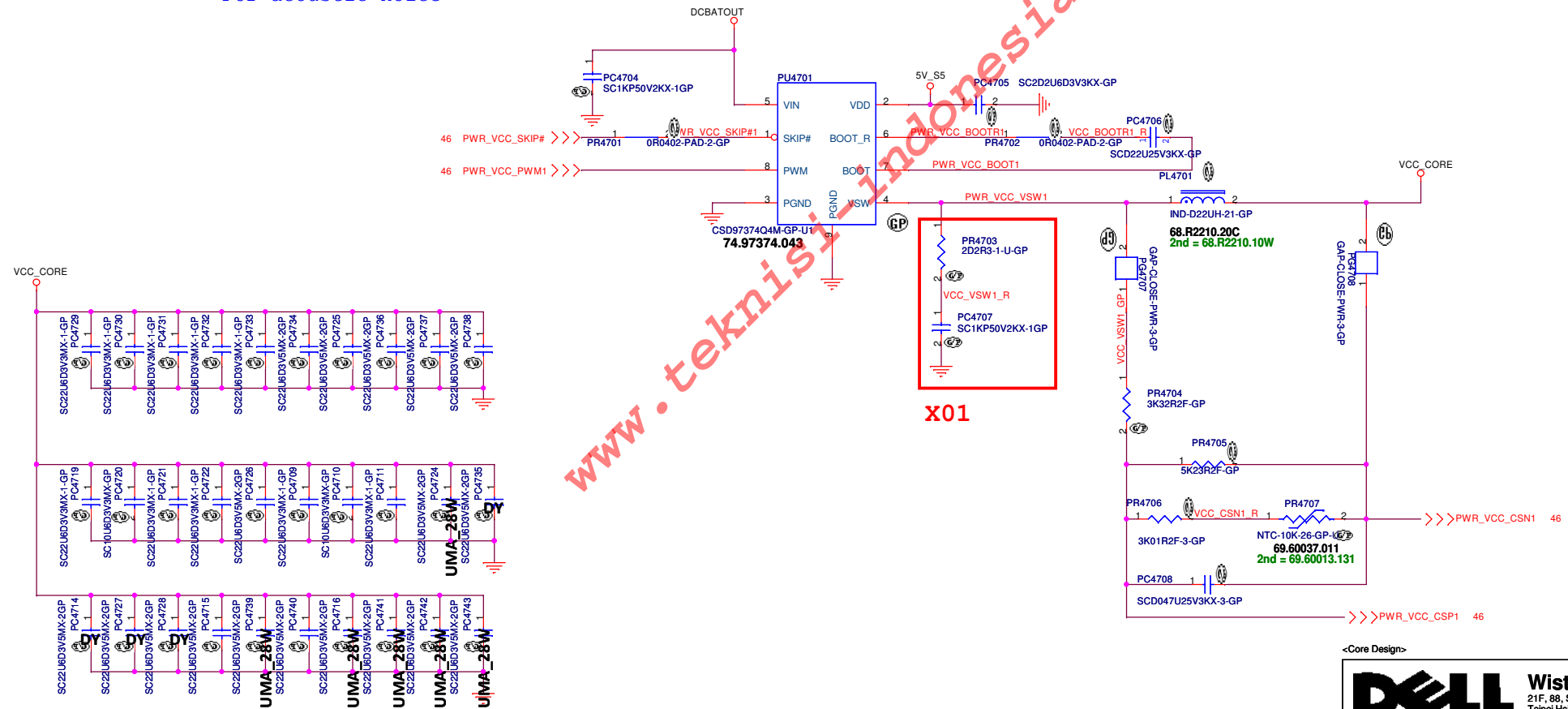
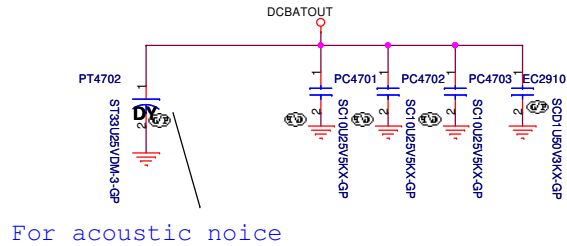
Design Current=5.894 A
8.841A<OCP>10.6A



I/P cap: CHIP CAP C 10 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI412DN-T1-GE3 / 24mohm/30mOhm4.5Vgs / 84.00412.037
L/S:SI406DN-T1-GE3 / 11.5mOhm/14.5mOhm4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 3.0U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH P63M063T-3R3MN Cyntec 28mhm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI5412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 64.00412.037
L/S:SI5406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 64.00406.037


```
SSID = CPU.Regulator
```



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Title

TPS51624 CPUCORE(2/2)

Size	A3
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Document Number

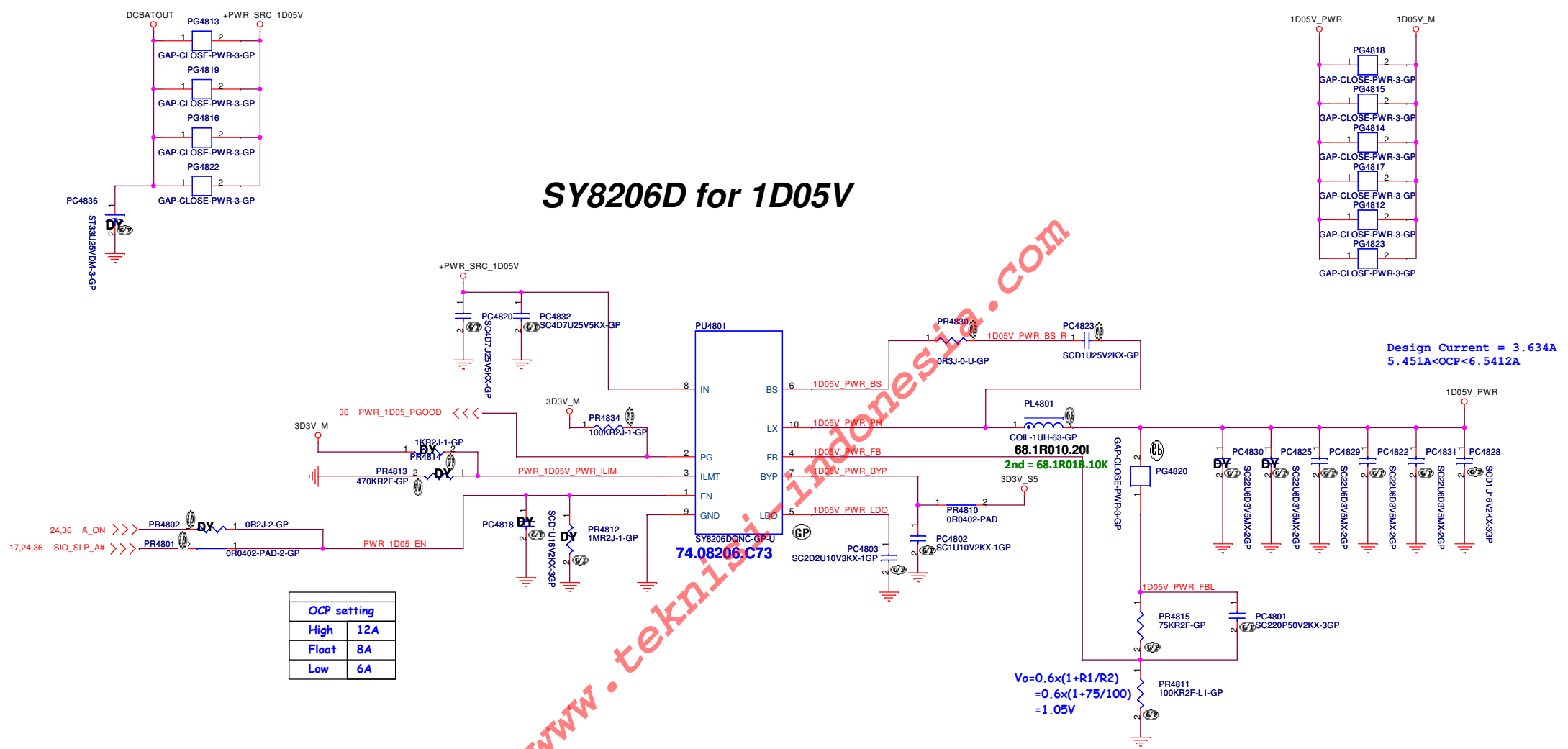
Round Rock MLK 13.3"

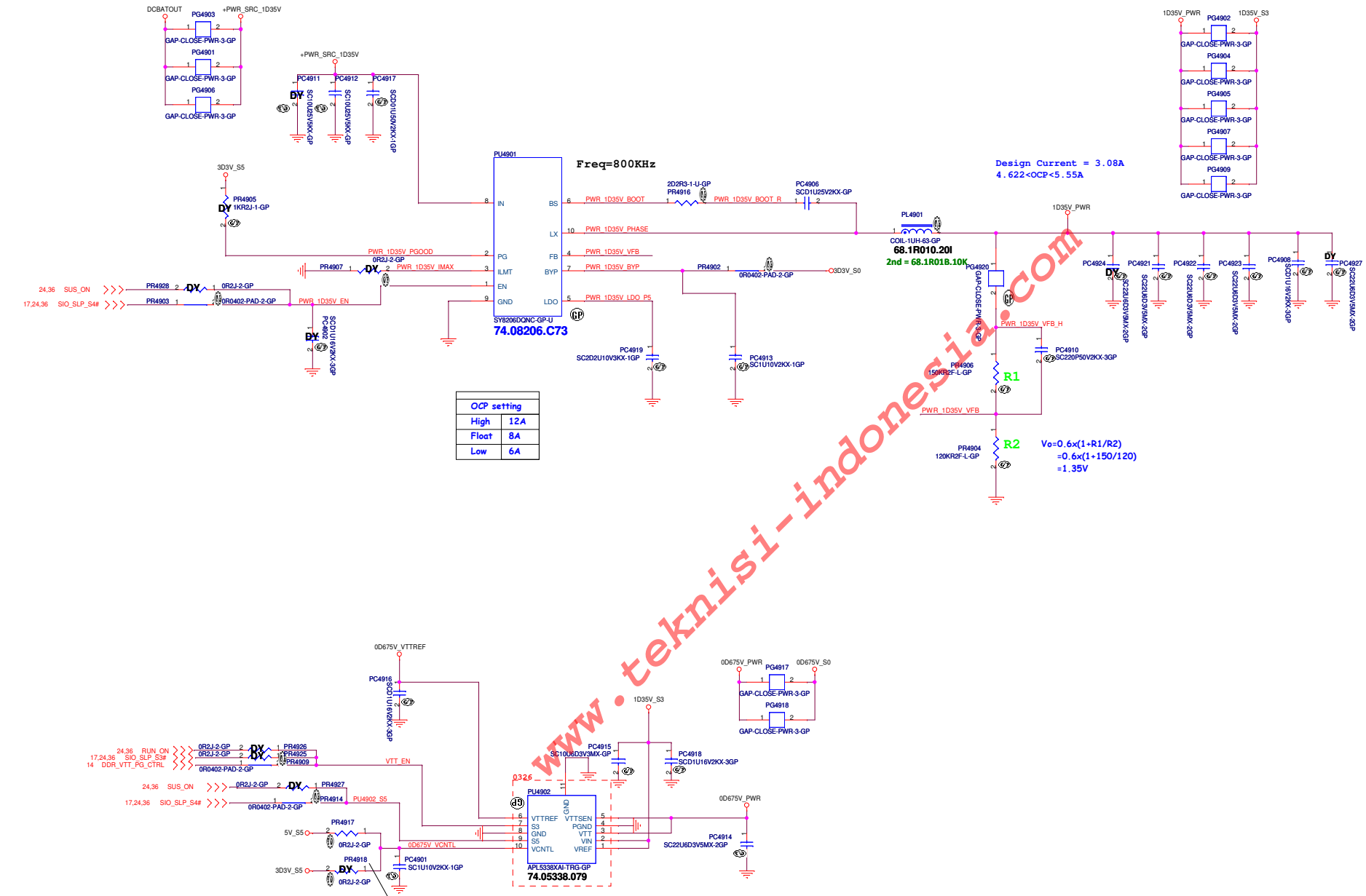
Rev
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SSID = PWR.Plane.Regulator_1p05v






OCP setting	
High	12A
Float	8A
Low	6A

If use 74.02997.B79, Stuff PR4918 and Dummy PR4917.

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Title			
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Size	Document Number		Rev
A4	Round Rock MLK 13.3"		
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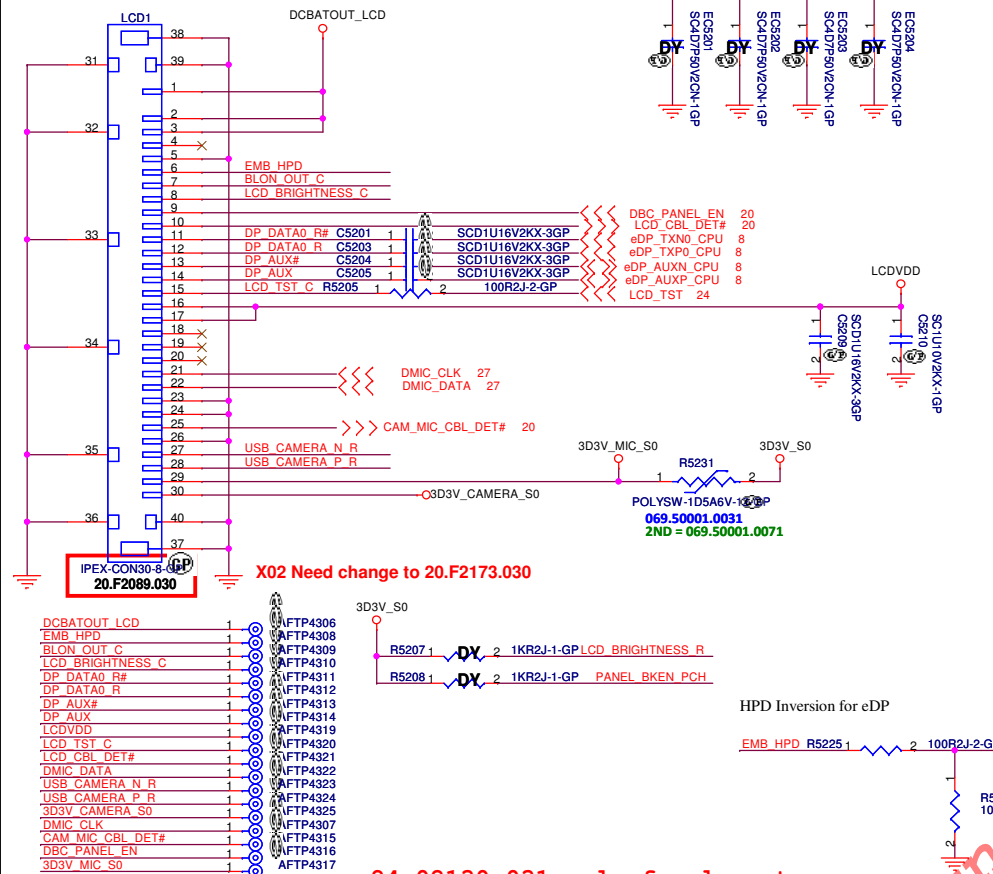
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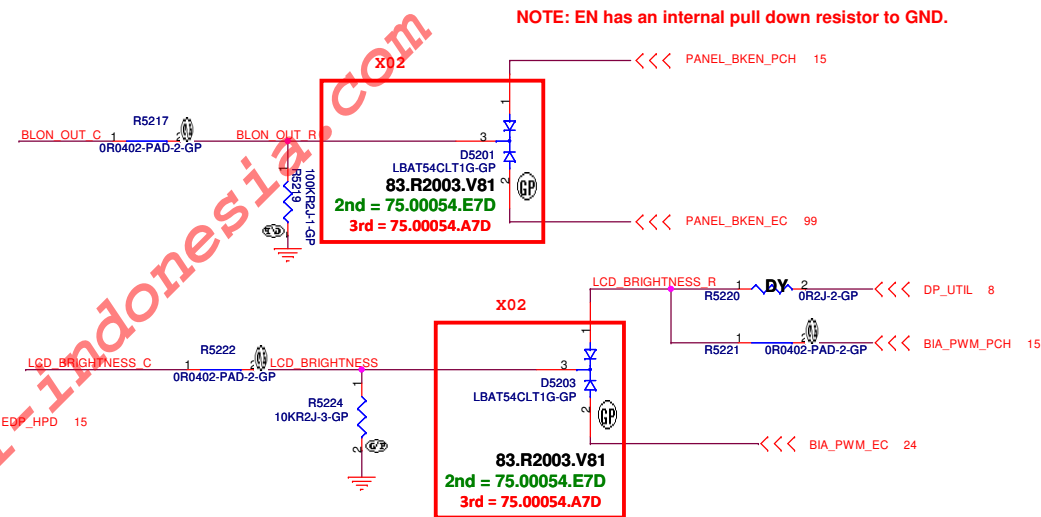
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Reserved			
Size A4	Document Number		Rev A00
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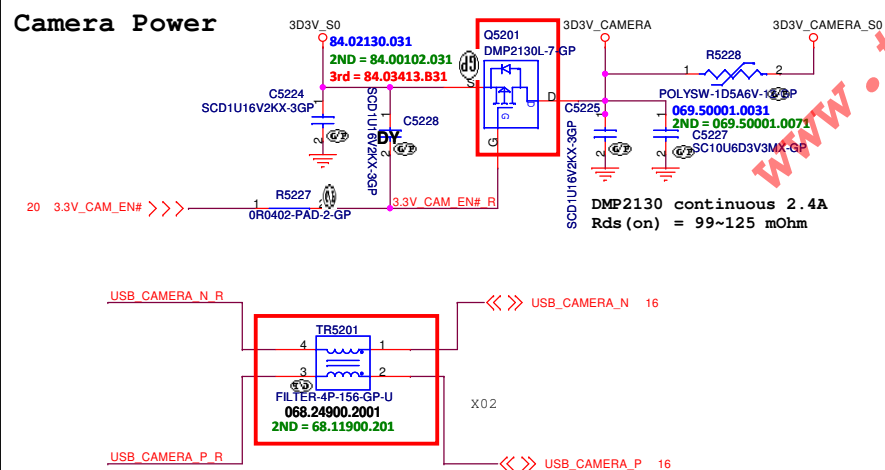
eDP CONNECTOR



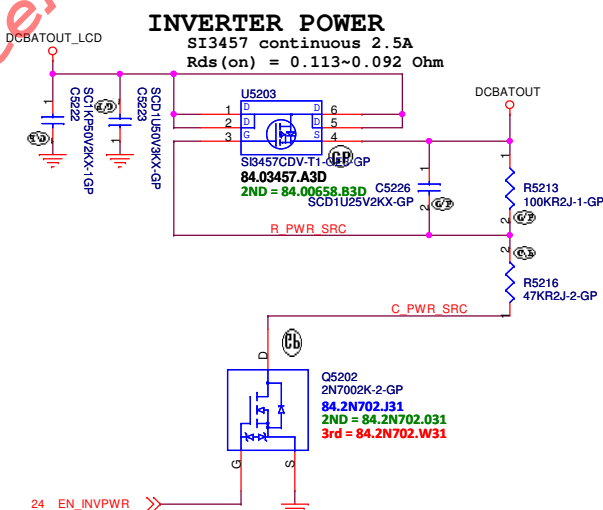
84.02130.031 only for layout



Camera Power



INVERTER POWER



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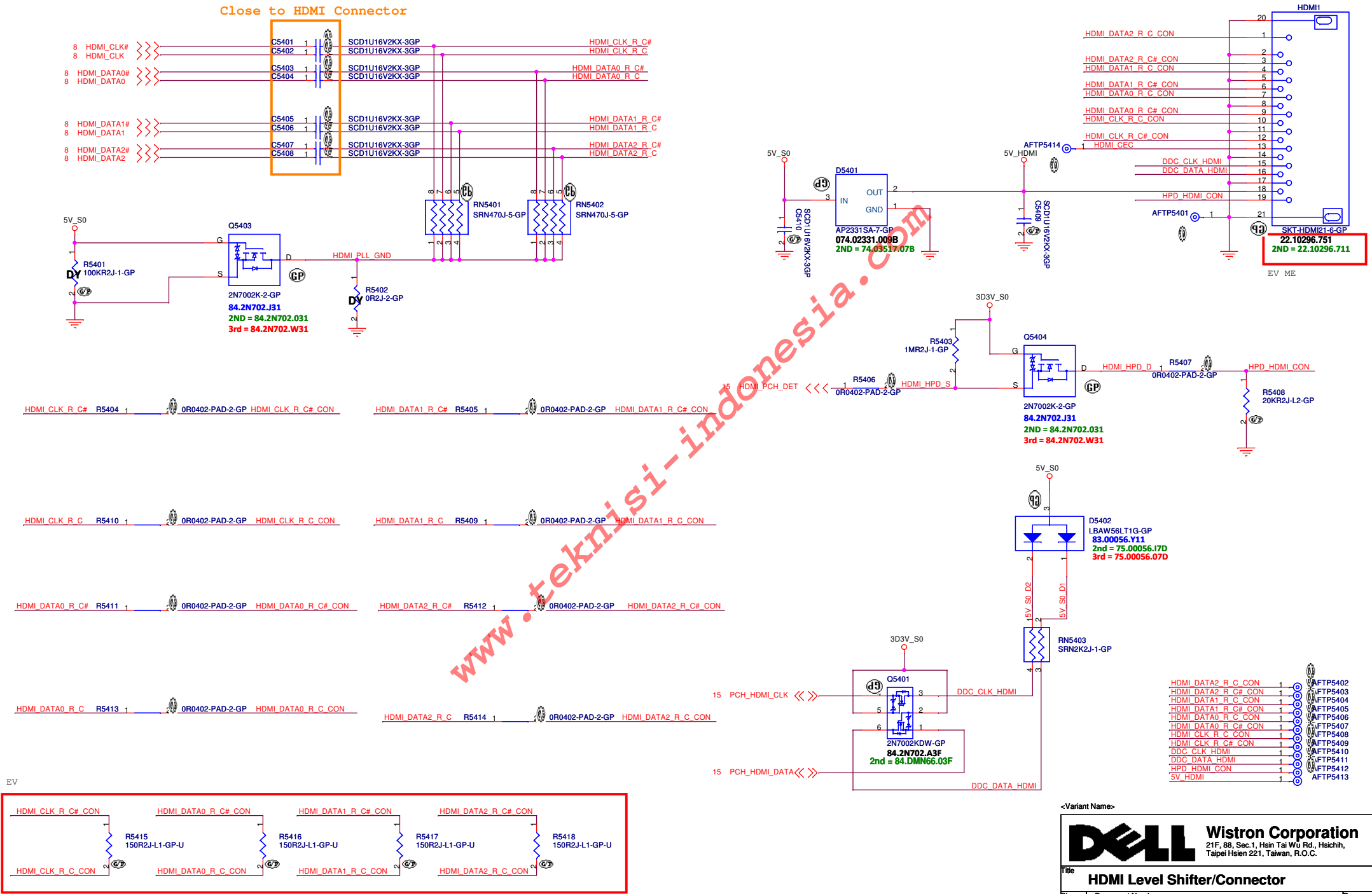
Date: Monday, August 17, 2015

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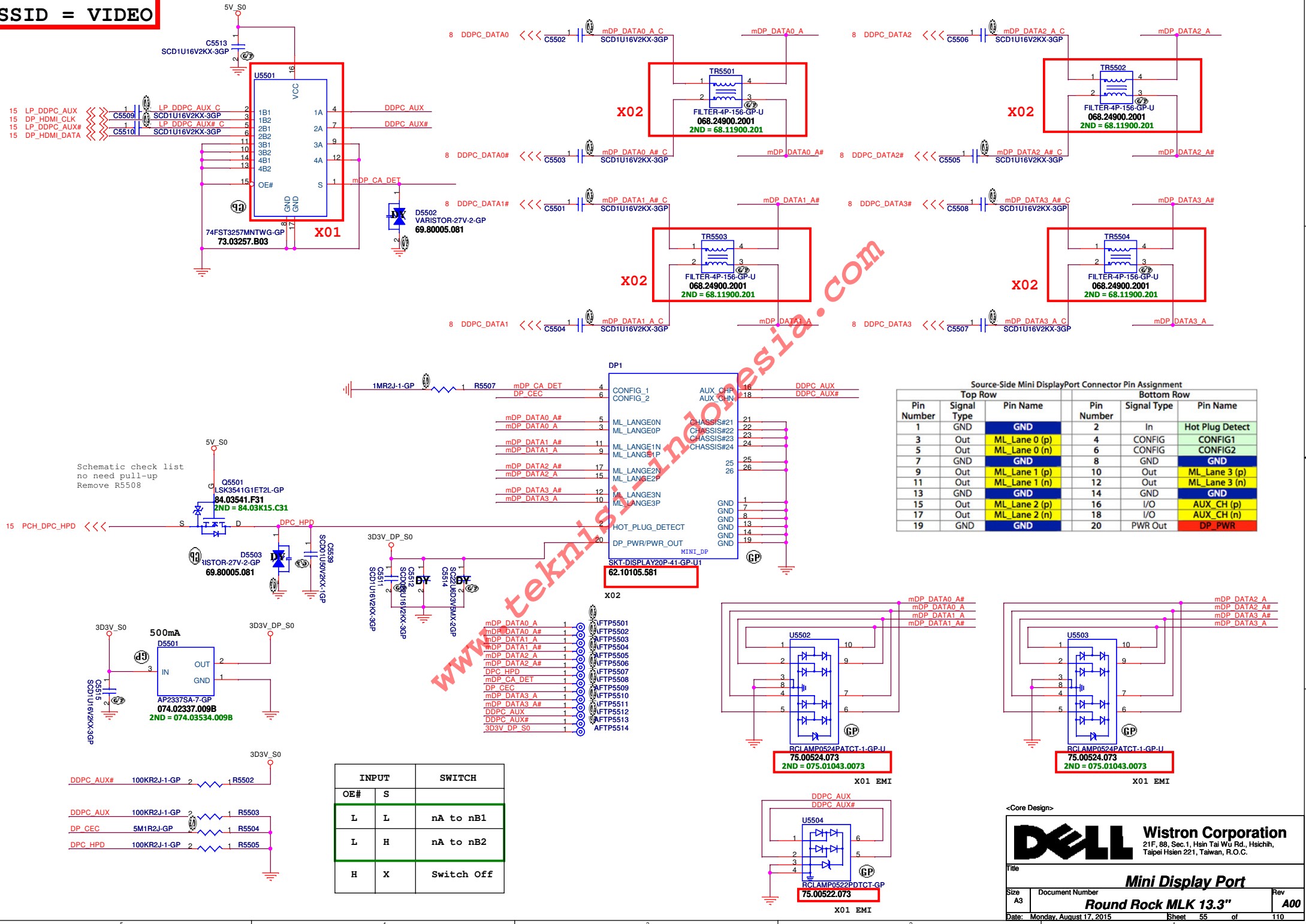
SSID = VIDEO

HDMI CONNECTOR

Close to HDMI Connector




SSID = VIDEO

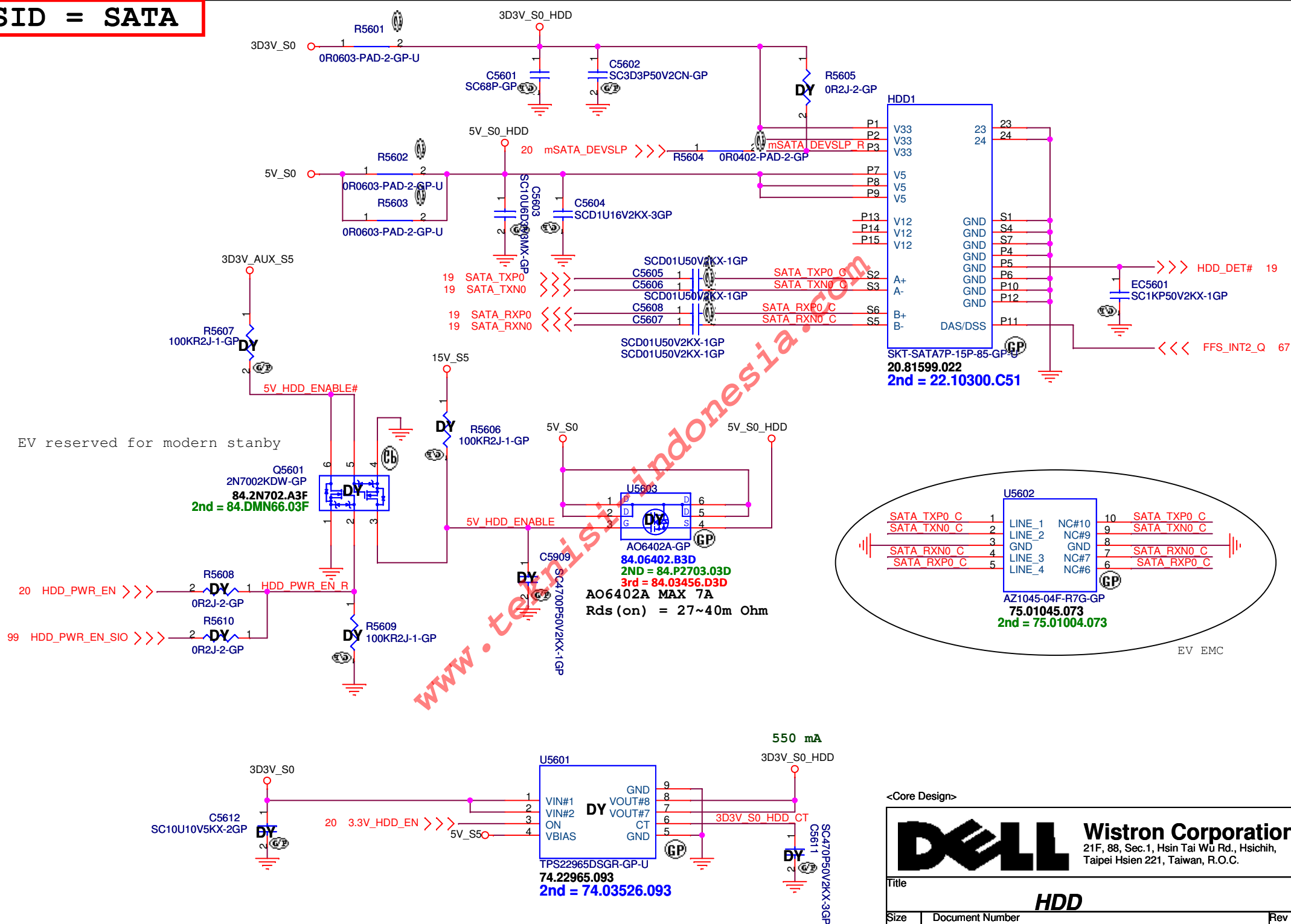


Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out	DP_PWR

INPUT		SWITCH
OE#	S	
L	L	nA to nB1
L	H	nA to nB2
H	X	Switch Off

<Core Design>			
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Title			
<i>Mini Display Port</i>			
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SSID = SATA



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Title

HDDSize
A4

Document Number

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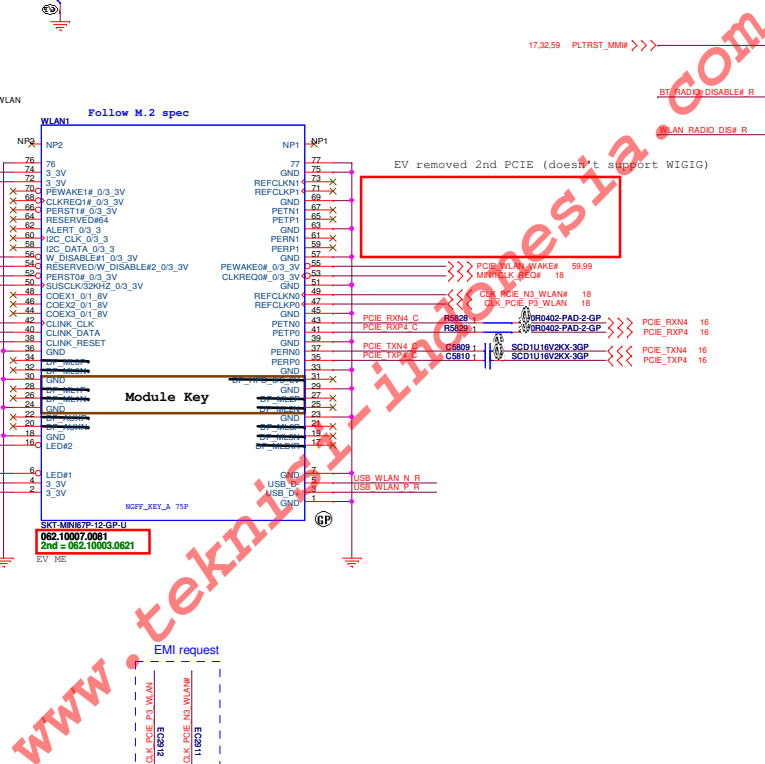
110

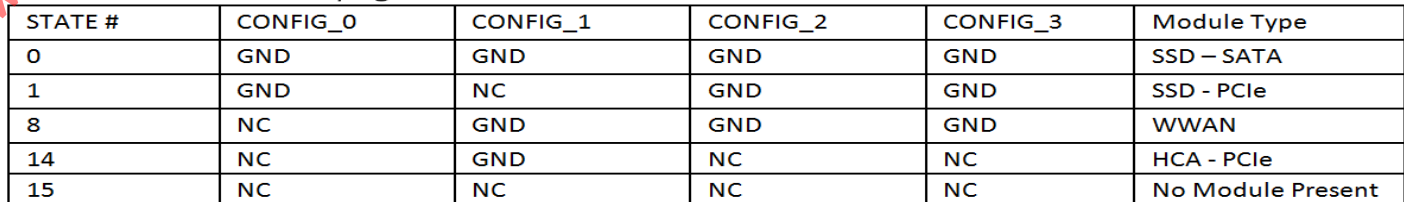
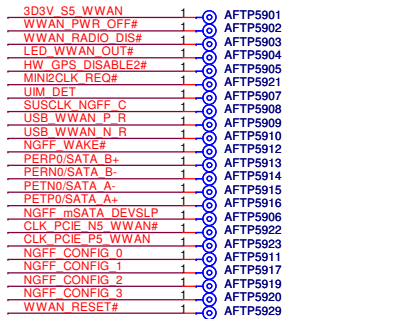
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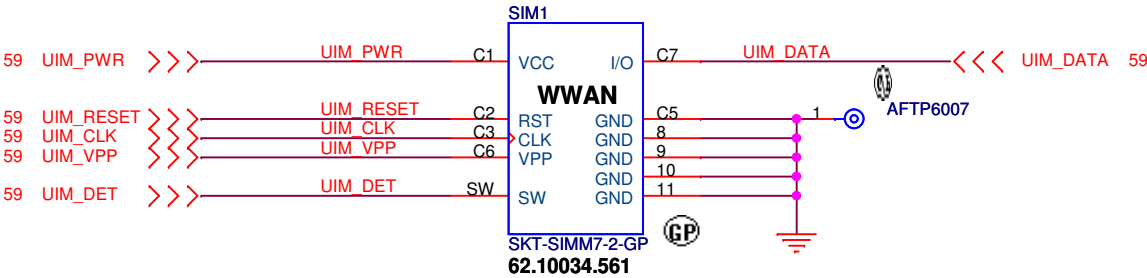
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Title			
Reserved			
Size A4	Document Number		Rev A00
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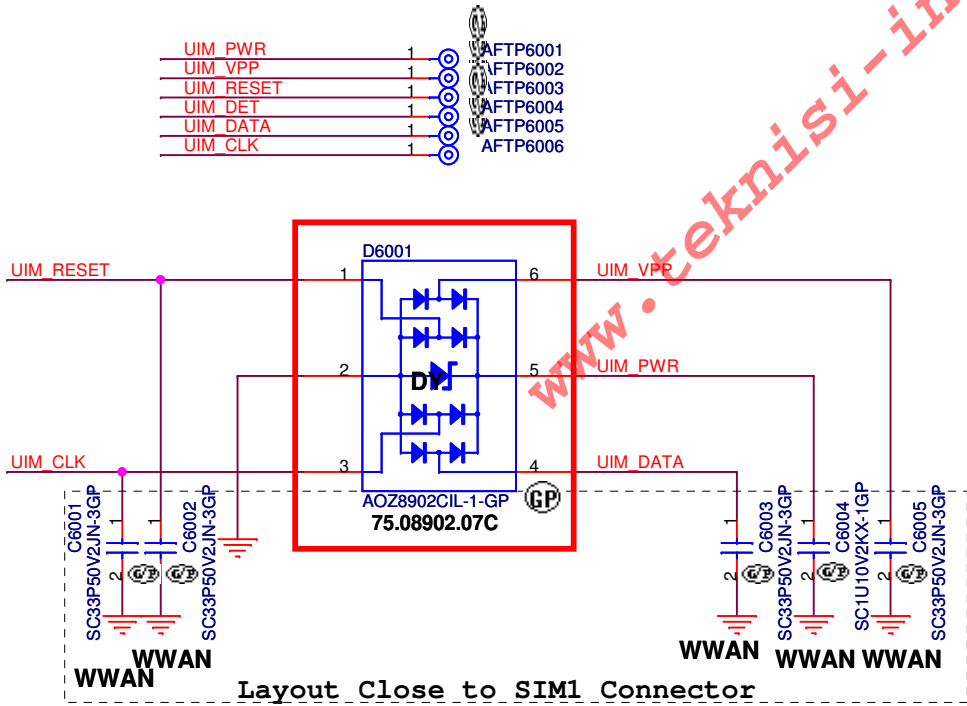
$$NGFF(WWAN/SSD)$$


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SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



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Title

uSIM

Size

Document Number

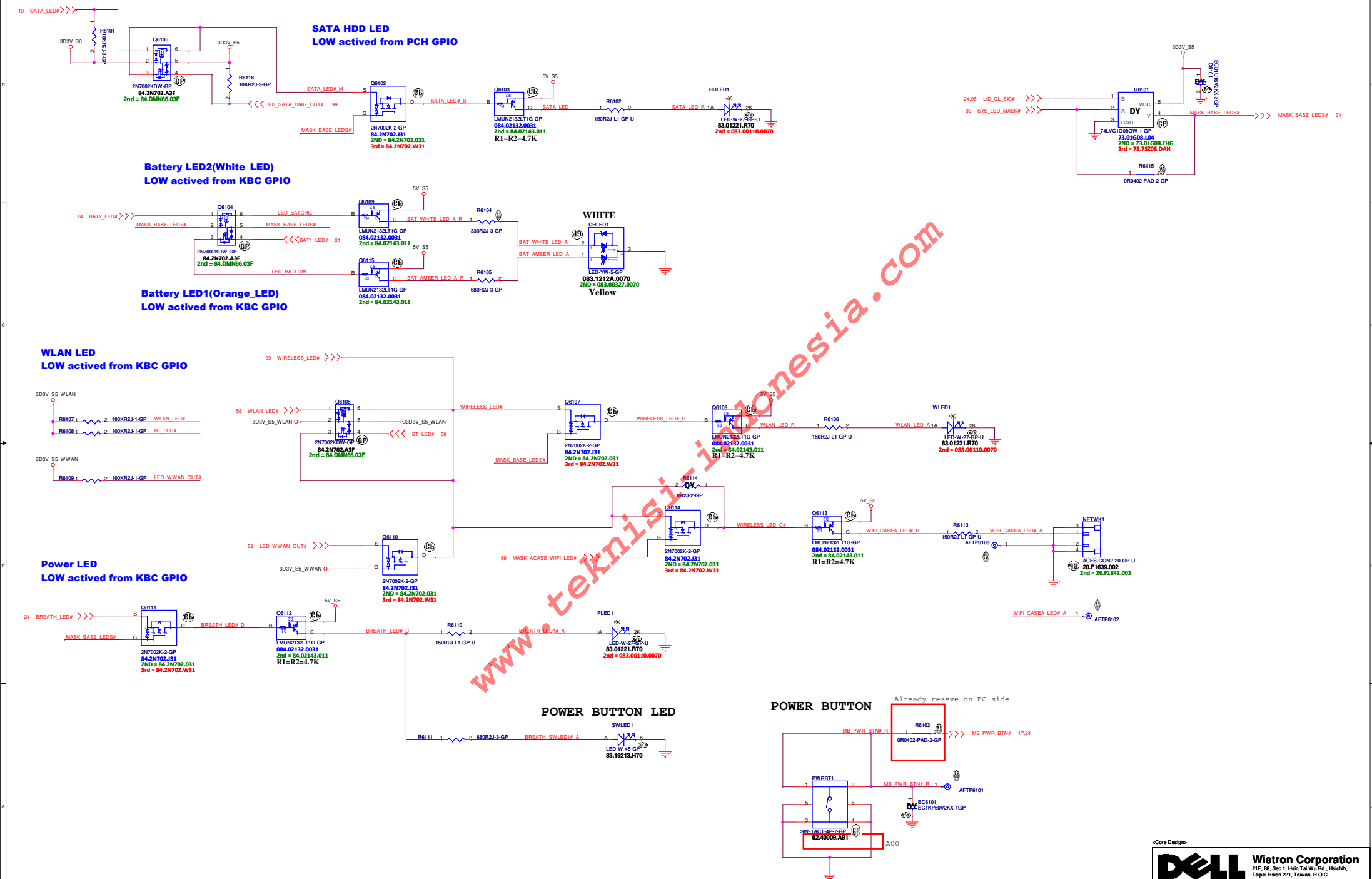
Rev

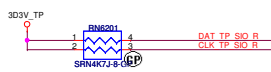
Round Rock MLK 13.3"

A00

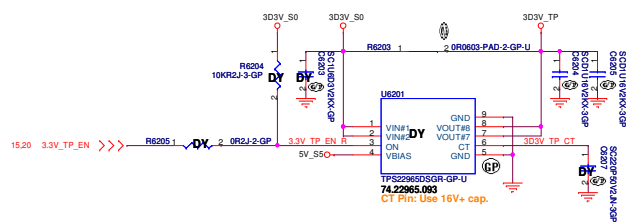
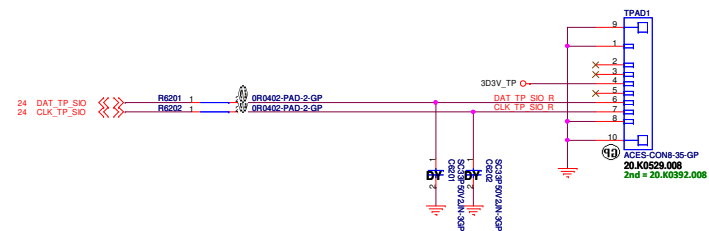
Date: Monday, August 17, 2015

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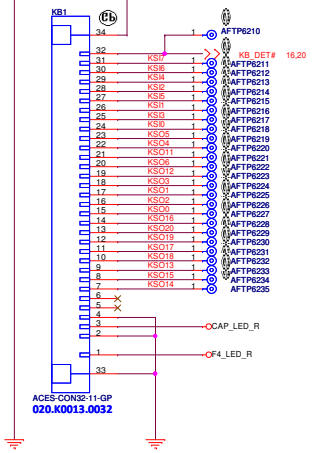


TouchPad Connector

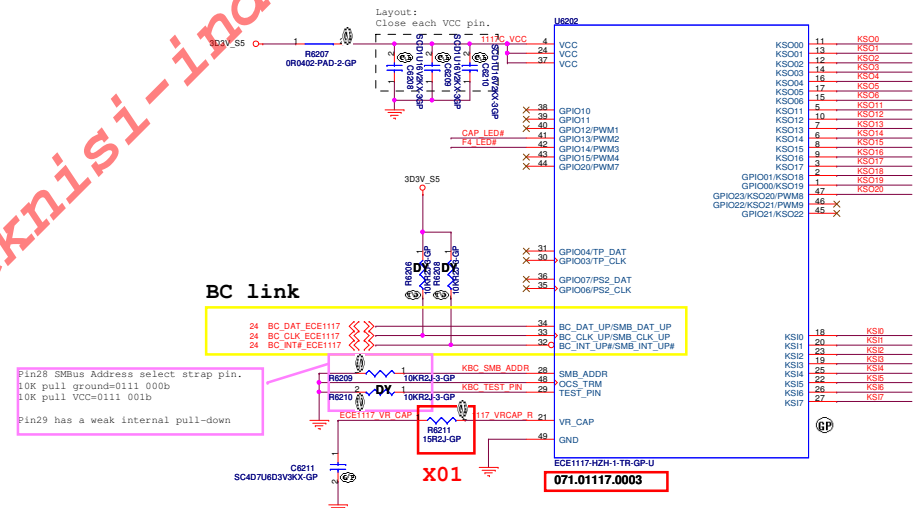


MB Pin NO.	Description	Module Pin NO.
32	Diagnostic	1
31	KSI[7]:S8	2
30	KSI[6]:S7	3
29	KSI[4]:S5	4
28	KSI[2]:S3	5
27	KSI[5]:S6	6
26	KSI[1]:S2	7
25	KSI[3]:S4	8
24	KSI[0]:S1	9
23	KSO[5]:D6	10
22	KSO[4]:D5	11
21	KSO[11]:D8	12
20	KSO[6]:D7	13
19	KSO[12]:D9	14
18	KSO[3]:D4	15
17	KSO[1]:D2	16
16	KSO[2]:D3	17
15	KSO[0]:D1	18
14	KSO[16]:D13	19
13	KSO[20]:D17	20
12	KSO[19]:D16	21
11	KSO[17]:D14	22
10	KSO[18]:D15	23
9	KSO[13]:D10	24
8	KSO[15]:D12	25
7	KSO[14]:D11	26
6	NC	27
5	NC	28
4	GND	29
3	Caps Lock LED	30
2	GND	31
1	F4 LED	32

Internal Keyboard Connector

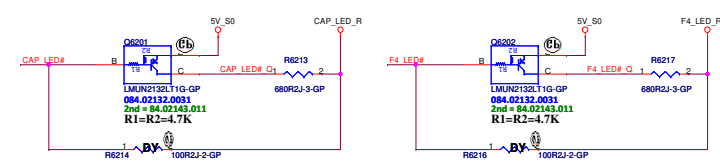


KBC SMSC ECE1117c



BC link

Pin28 SMBus Address select strap pin.
10K pull ground=0111 000b
10K pull VCC=0111 001b
Pin29 has a weak internal pull-down



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Title

IO CONN

Size
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Document Number

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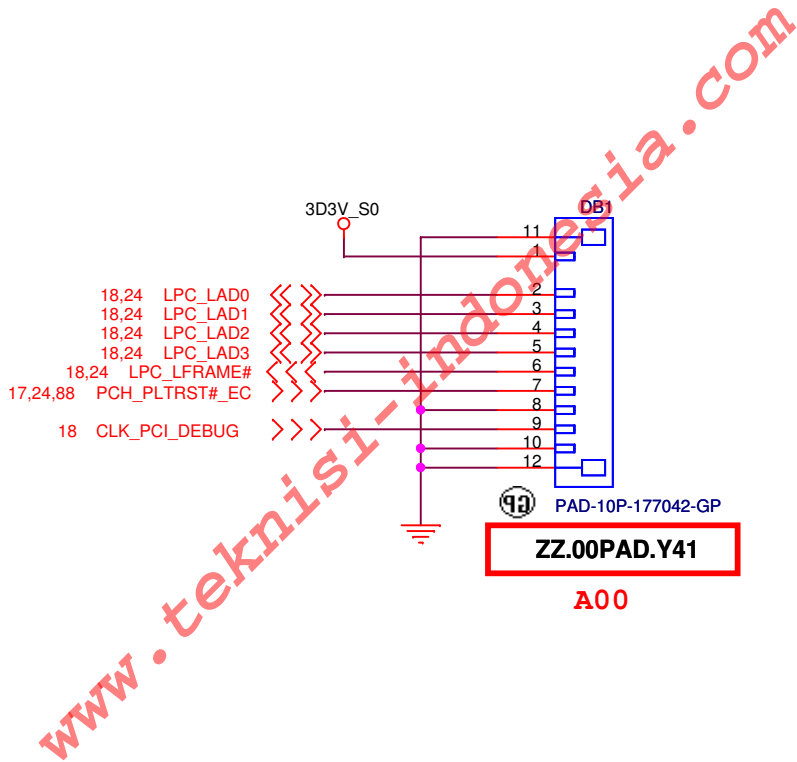
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Hall Sensor			
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SSID = DEBUG PORT




<Core Design>

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Title Debug connector			
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Title

SENSOR

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Title

Thunderbolt (1/5)

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Title

Thunderbolt (2/5)

Size
A

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Title

Thunderbolt (3/5)

Size
A

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Title

Thunderbolt (4/5)

Size
A

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Title

Thunderbolt (5/5)

Size
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Title

GPU (1/5) PEG

Size
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Title

GPU (2/5) DIGITAL

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Title

GPU (3/5) VRAM

Size
A

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Title

GPU (4/5) GPIO

Size
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Title		
GPU (5/5) PWR/GND		
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Title

VRAM1,2 (1/4)

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Title

VRAM3,4 (2/4)

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Title

VRAM5,6 (3/4)

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Title			
VRAM7,8 (4/4)			
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Title

VGA CORE

Size
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Title

DISCRETE VGAPOWER

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Title

Switchable GFXLCD

Size
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Document Number

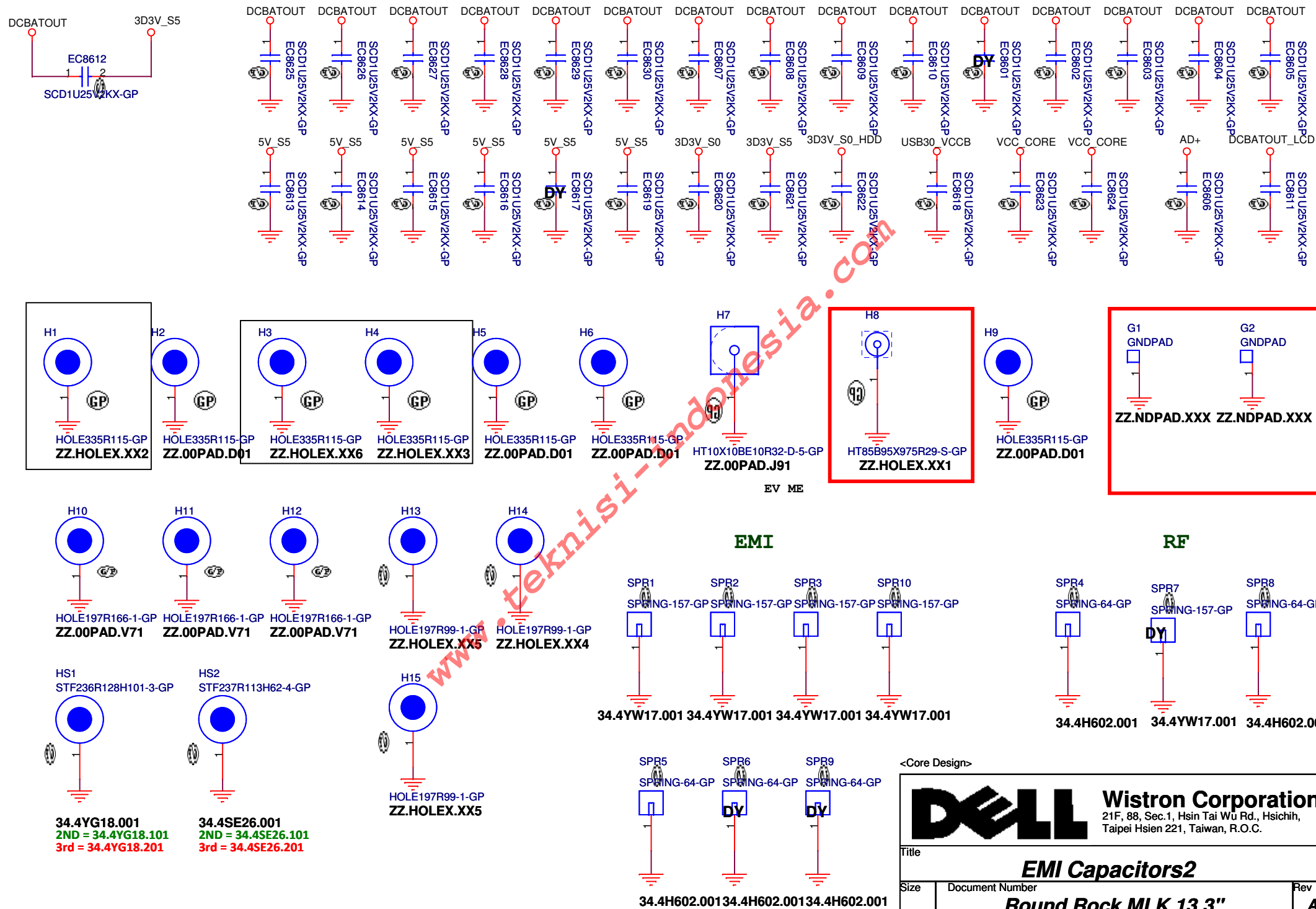
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SSID = USH

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<Variant Name>

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Title			
USH Board Connector			
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NFC Connector			
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Title Smart Card			
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Title

Reserved

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SSID = Docking

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Title DOCKING			
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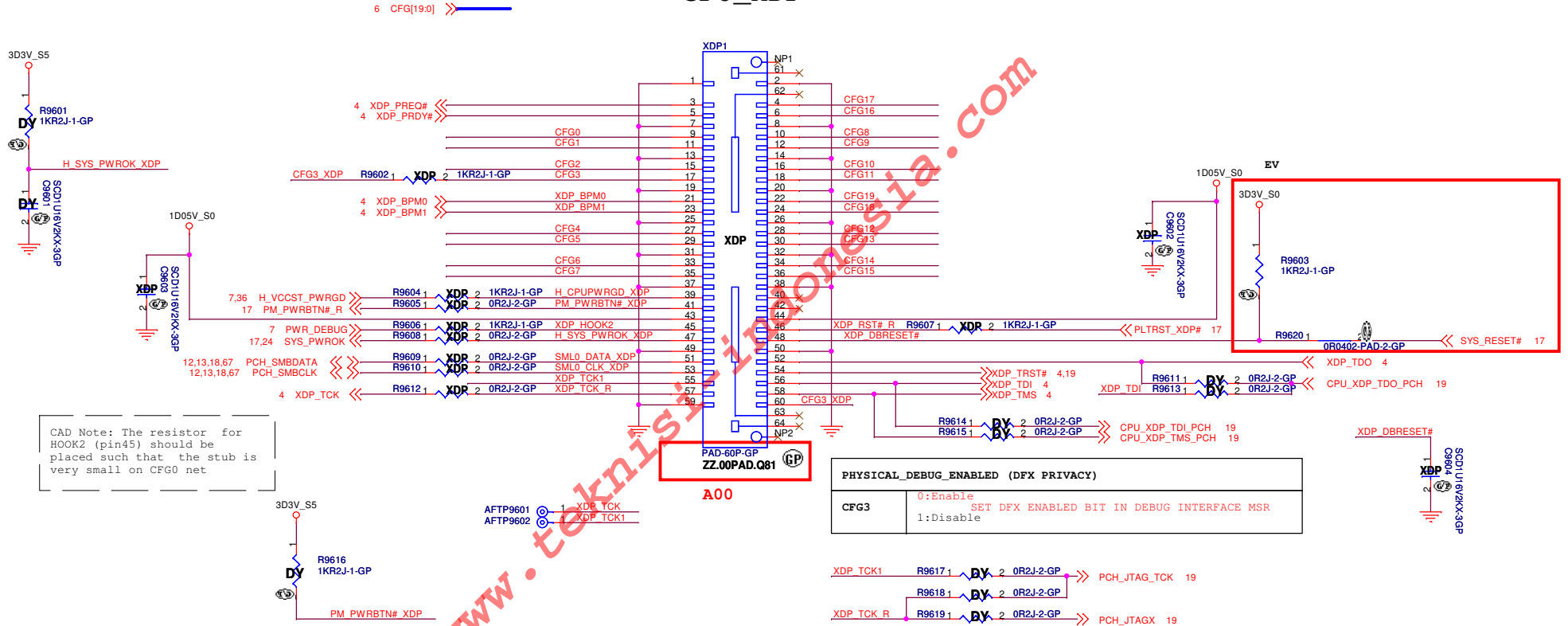
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Title			
LAN SW			
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SSID = CPU_XDP

CPU_XDP




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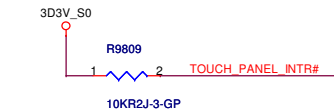
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Title			
USB2.0 HUB			
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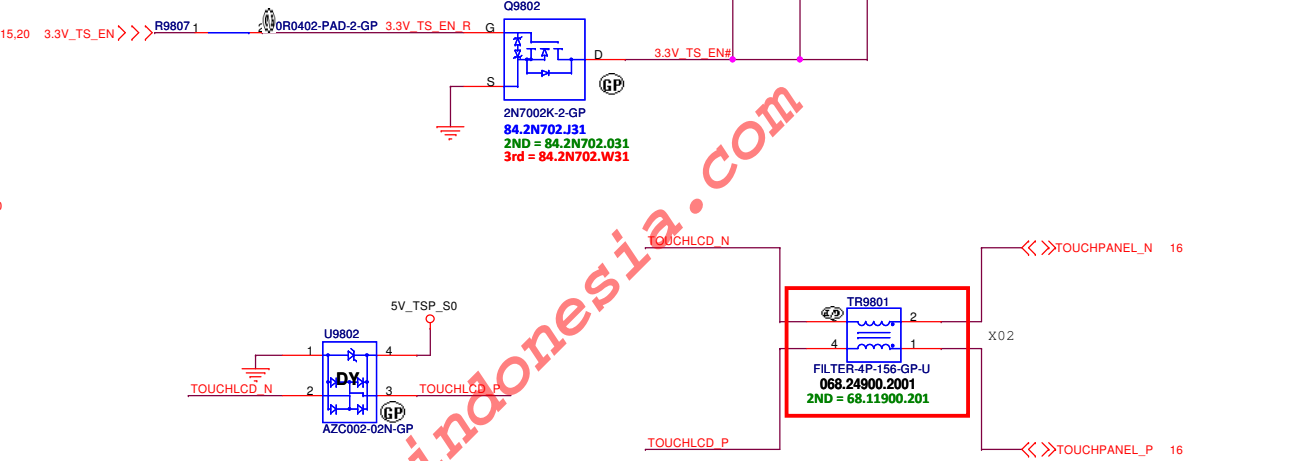
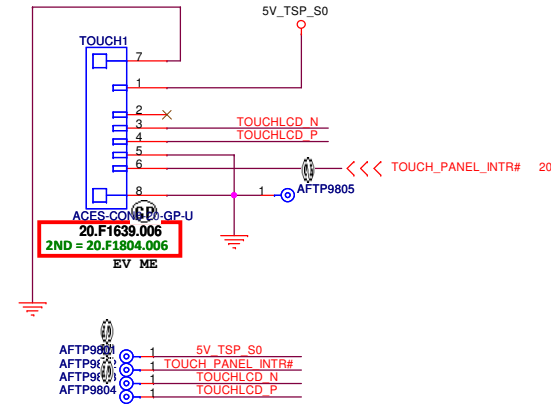
SSID = User.Interface

TOUCH PANEL POWER

84.02130.031 only for layout

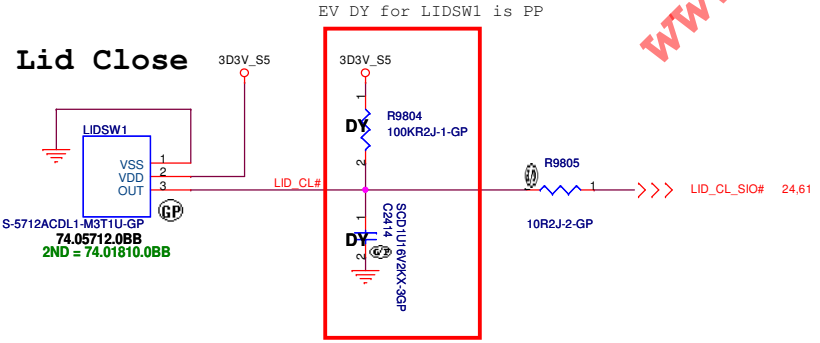


TOUCH PANEL CONNECTOR



EV follow ARD

Lid Close



ME FWP_EC R9802 1 2 0R2J-2-GP ME FWP

Install after MP

Firmware SW

24 ME_FWP_EC >>>

19 ME_FWP <<<

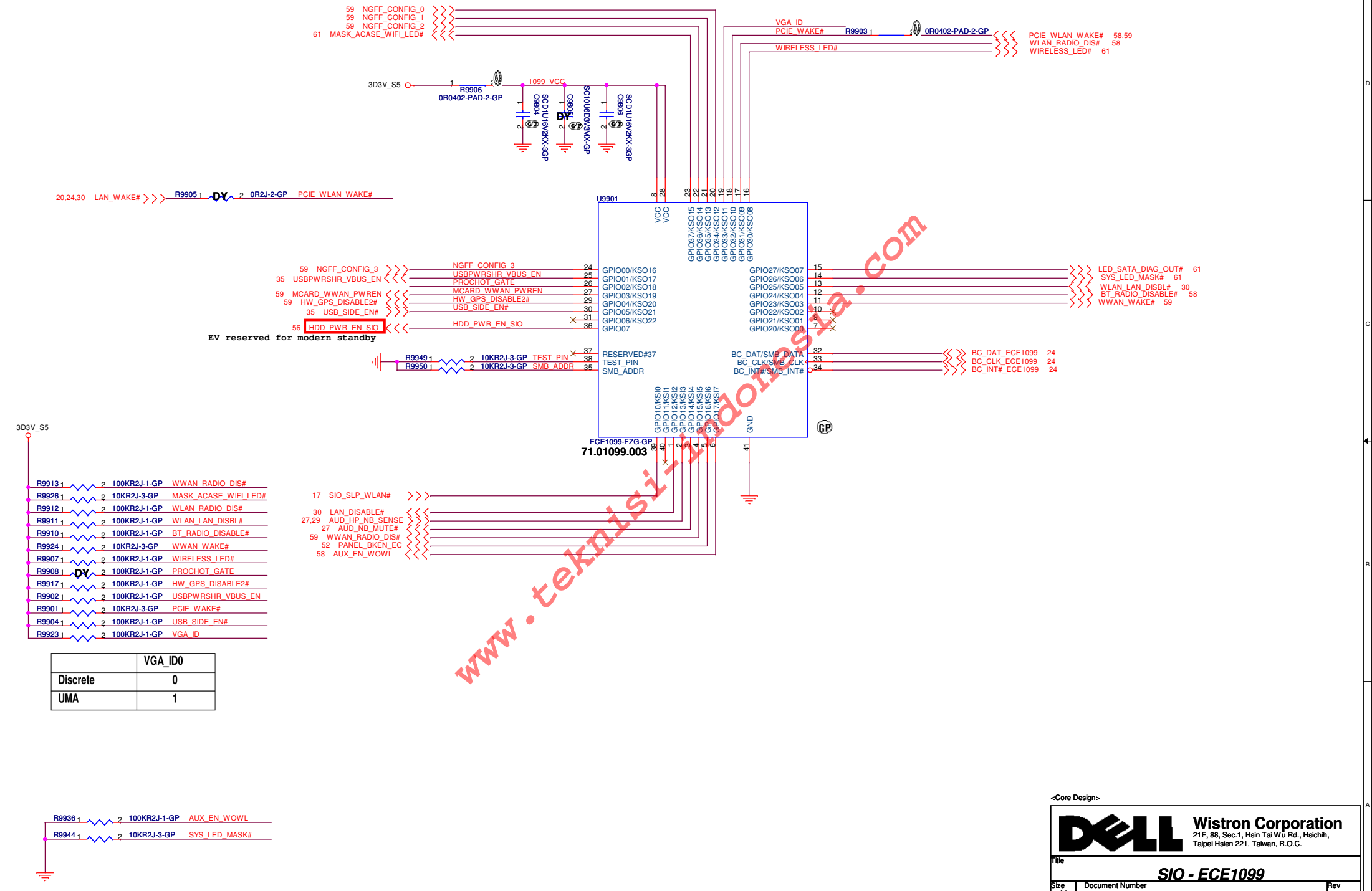
3D3V_S5_PCH R9812 2 1 1KR2J-1-GP

MESW1

SW-SLIDE6P-6-GP 62.40018.691

	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

SSID = SIO



	VGA_ID0
Discrete	0
UMA	1

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Title			SIO - ECE1099		
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Processor Strapping

Name	Strap Description	Schematics Notes
CFG[0]		Connect a series 1 k resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort. No connect for disable. 0:Enabled - An external Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1KΩ ± 5% resistor to enable port.
SPKR/GPIO81	No Reboot on TCO Timer expiration	This signal has an integrated weak pull-down (20KΩ nominal) to enable reboot on TCO Timer expiration. Pull up to VCC3_3 through a 1K to 8.2KΩ ± 5% resistor to disable this capability.
SDIO_D0/GPIO66	Top-Block Swap Override	This signal has an integrated weak pull-down (20KΩ nominal) resistor to disable Top-Block Swap mode. To enable Top-Block Swap, this signal should be pulled up to VCCSDIO through a 1K to 4.7KΩ ± 5% resistor. The reference voltage for this strap is VCCSDIO.
INTVRMEN	Integrated VRM Enable/Disable	This signal has no integrated pull-up/pull-down resistor. To enable the integrated voltage regulator for DCPSUS1, DCPSUS2, DCPSUS3 and DCPSUS4 this signal must be pulled to VCCRTC through a weak resistor (e.g.330KΩ ± 5%). To disable the integrated voltage regulator, this signal must be pulled down through a weak resistor (e.g. 330KΩ ± 5%) and the DCPSUS rails must be powered externally.
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable boot from SPI. To enable boot to LPC this signal must be pulled up to VCC3_3 through a 1K to 8.2KΩ ± 5% resistor.
HDA_SDO/I2S0_TXD	Flash Descriptor Security Override	This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable security measures in the flash descriptor. To enable Flash Descriptor Security Override this signal must be pulled up to VCCHDA through a 1K to 4.7KΩ ± 5% resistor.
GPIO15	TLS Confidentiality	This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. To enable Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality this signal must be pulled up to VCCSUS3_3 through a 1K to 8.2KΩ ± 5% resistor.
DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1K to 3.6KΩ ± 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1K to 3.6KΩ ± 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	This signal has no integrated pull-up/pull-down. This signal must always be pulled to VCCRTC through a weak resistor (e.g. 330KΩ ± 5%).

USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2 (win debug)
2	WWAN
3	WLAN (BT)
4	N/A
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 MCP Side

Pair	Device
1	USB port 1
2	USB port 2
3	WWAN
4	N/A

PCIE Table

PCIE	
Lane	Device
1	NA
2	Card Reader
3	LOM
4	WLAN
5	NA
6	NA

SATA Table

SATA	
Pair	Device
0	HDD
1	NA
2	NA
3	NGFF WWAN

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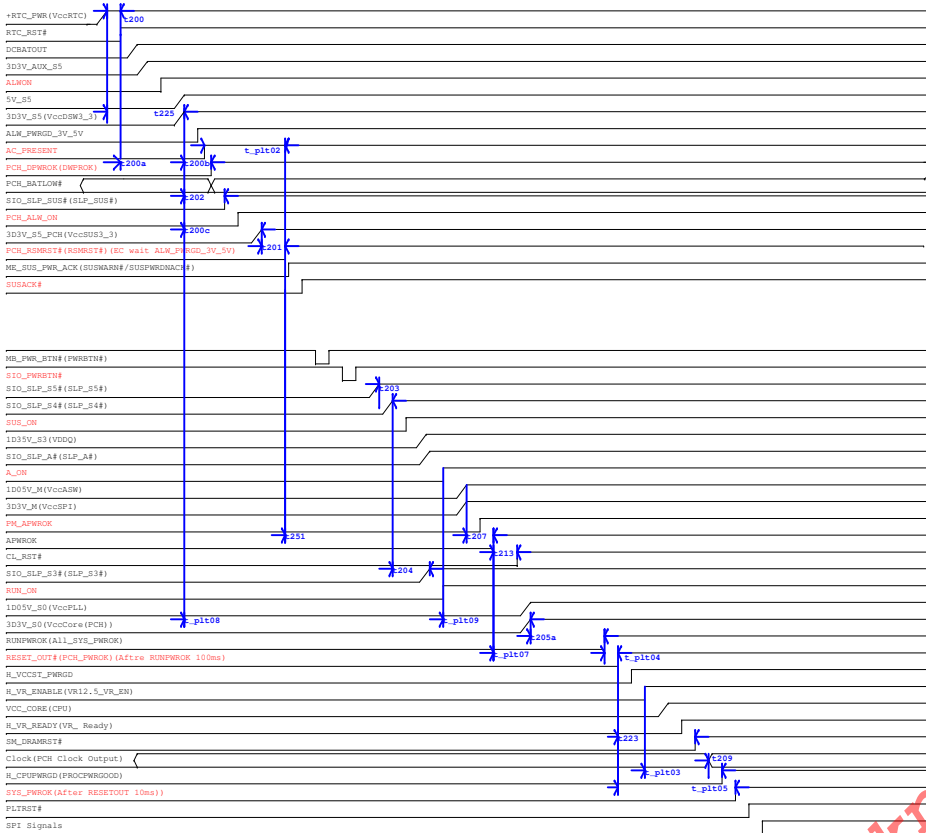
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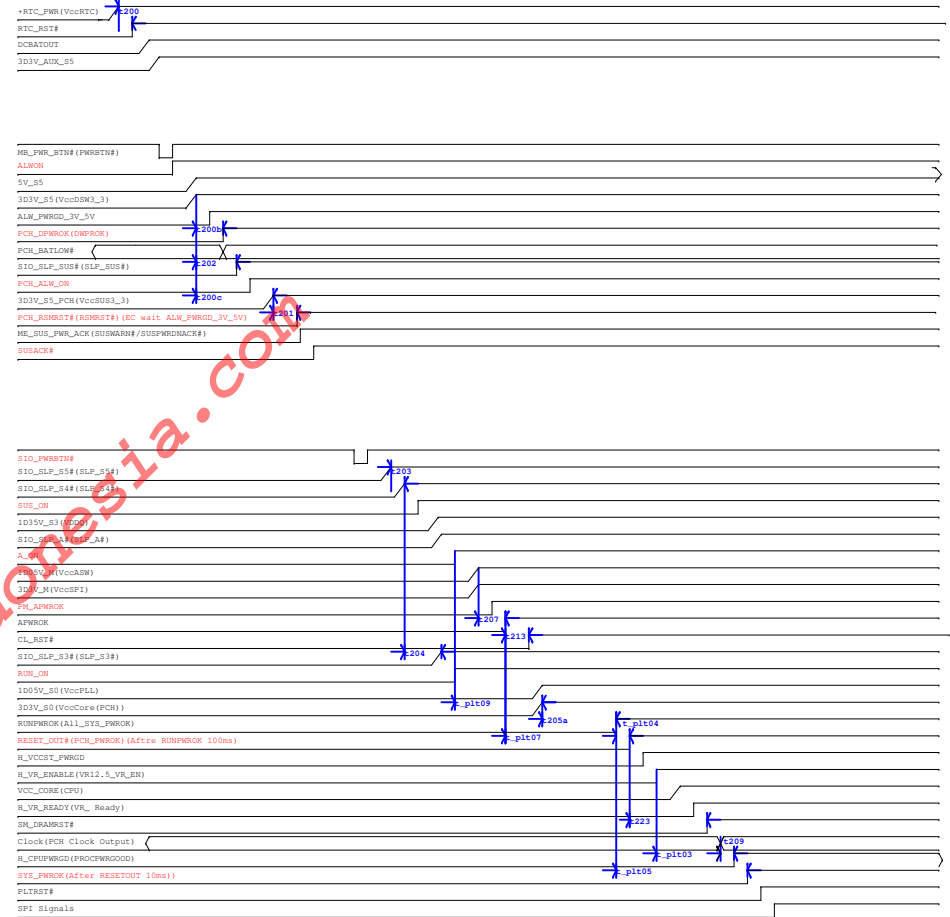
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Intel-Power Up Sequence

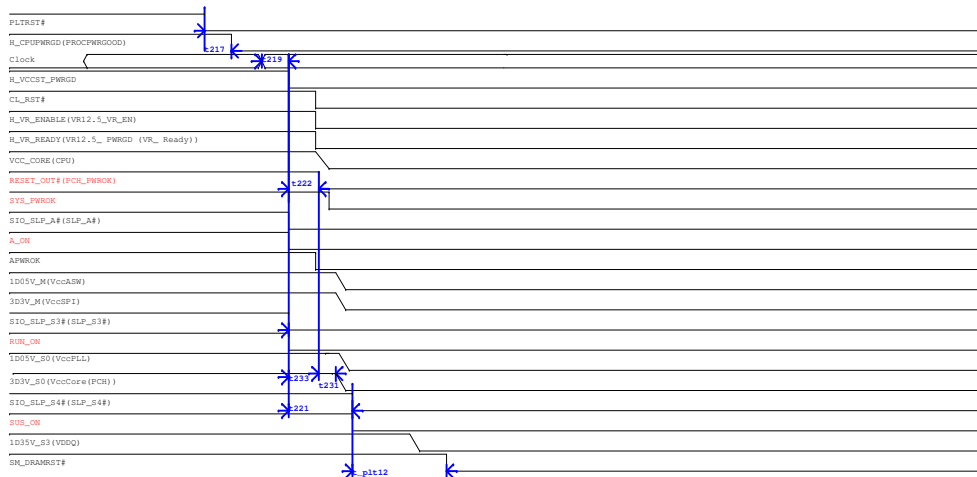
(AC mode) Red word: KBC GPIO

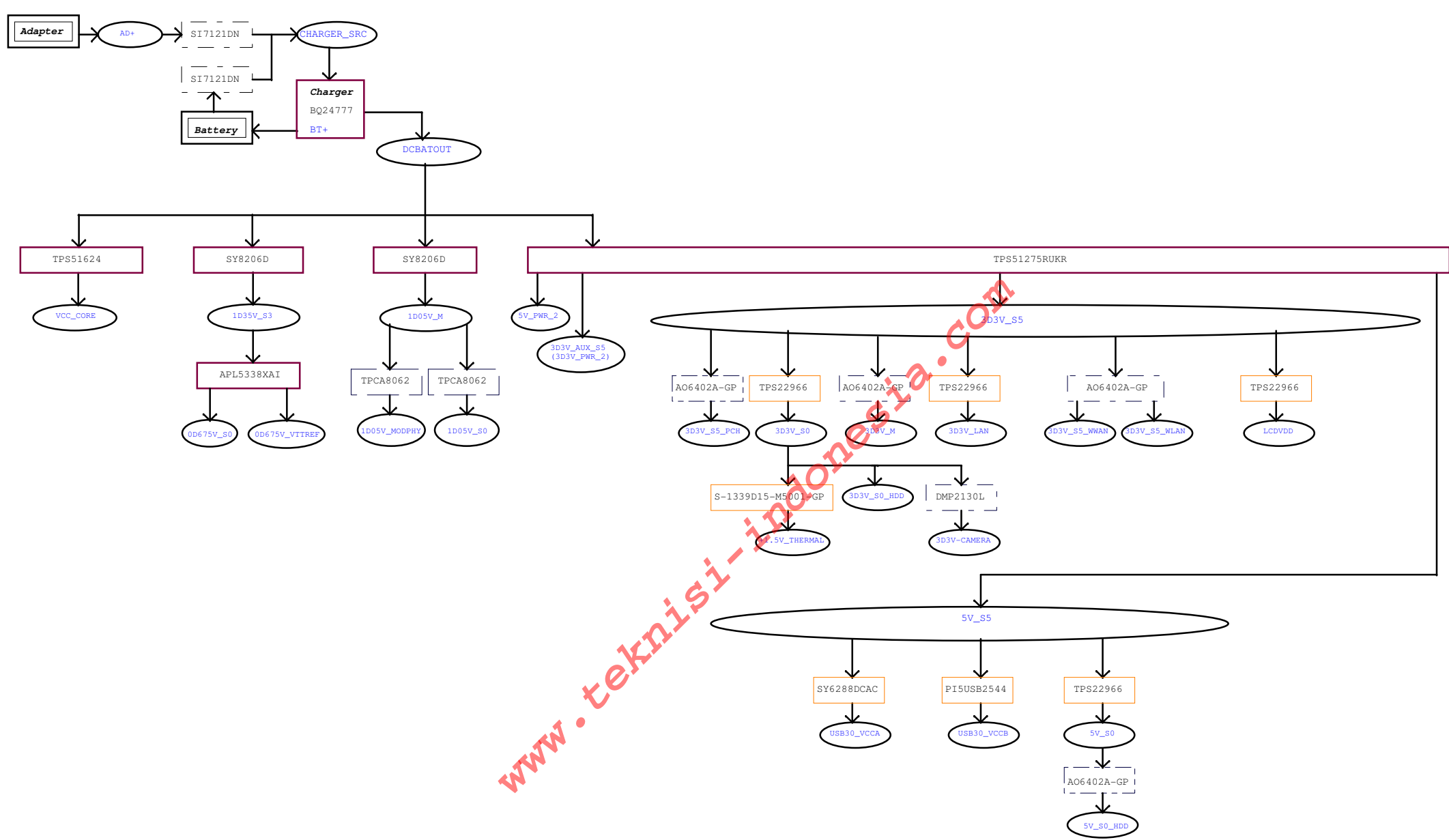


(DC mode) Red word: KBC GPIO

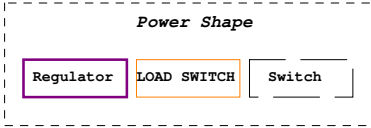


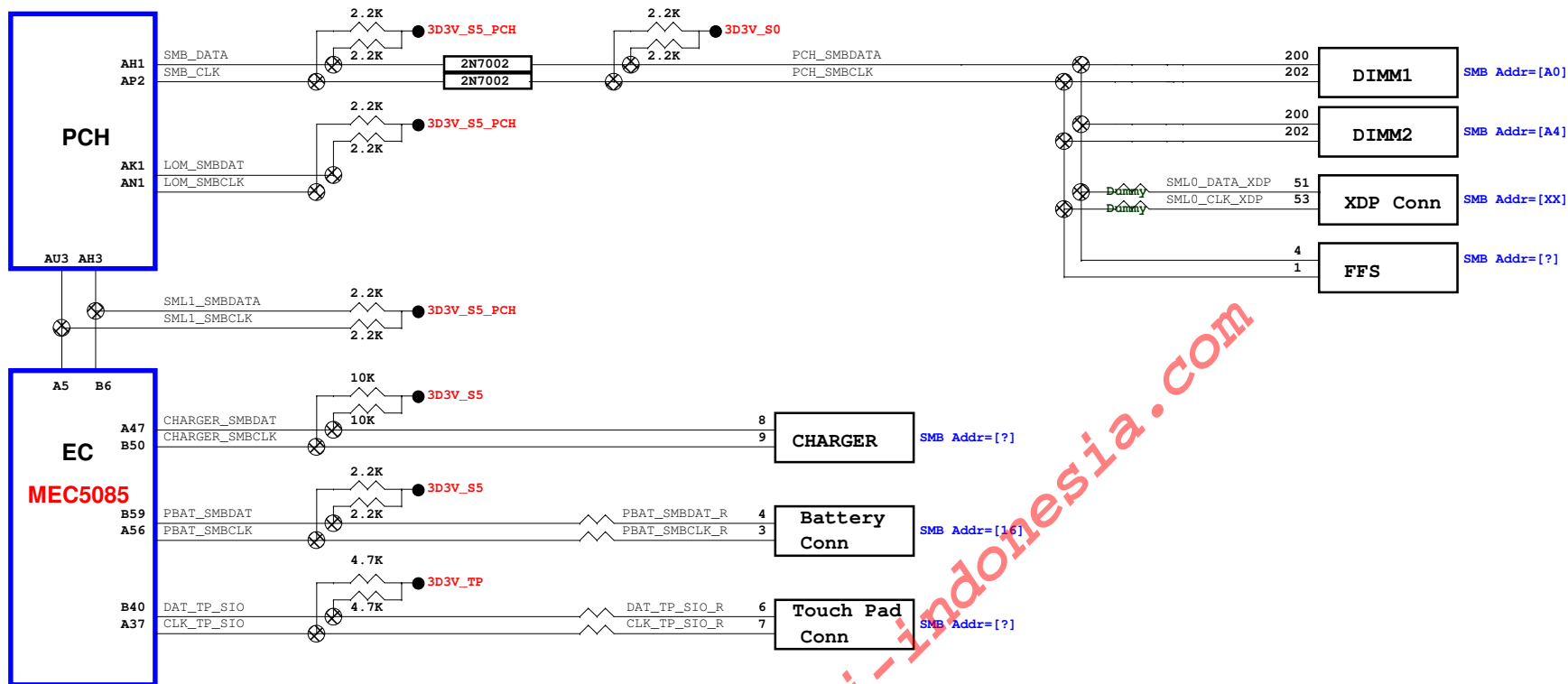
(AC mode) red word: KBC GPIO





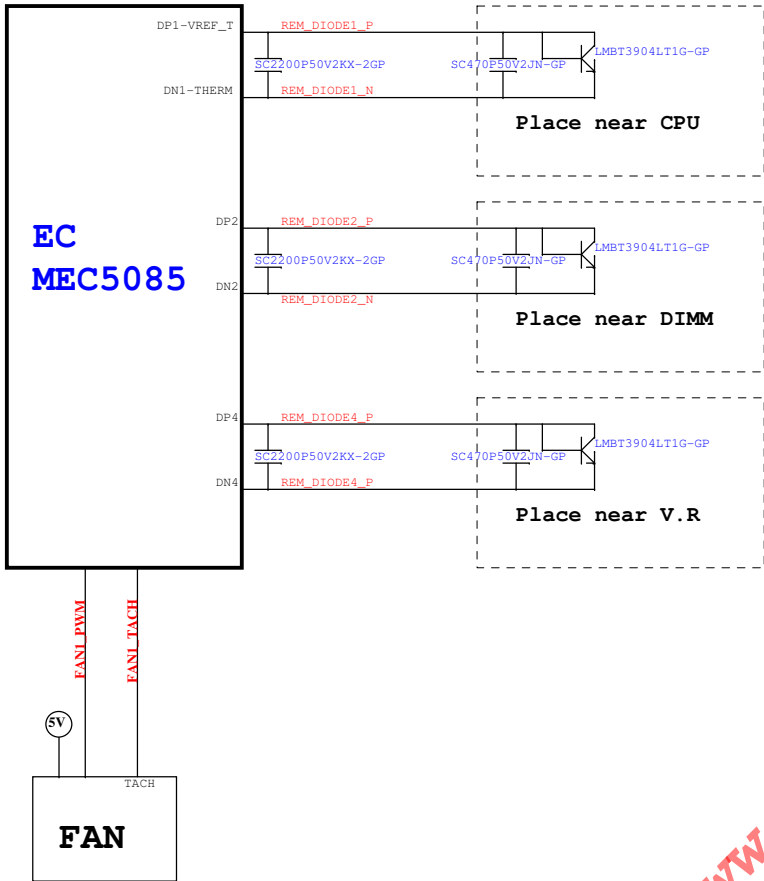
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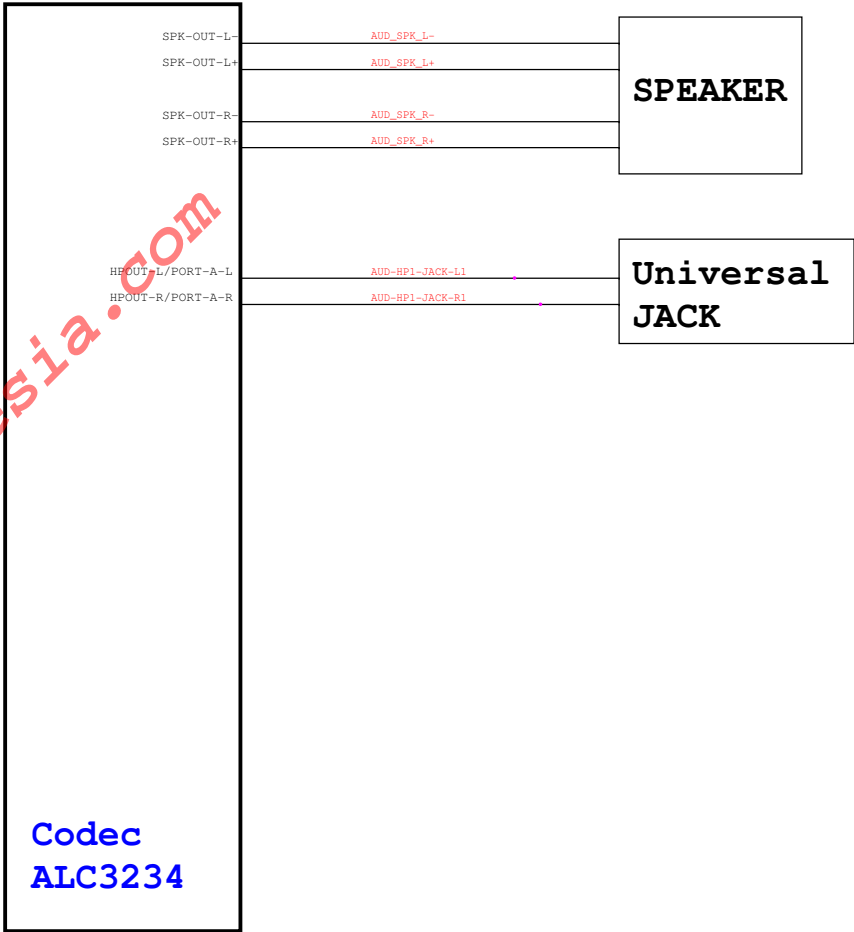


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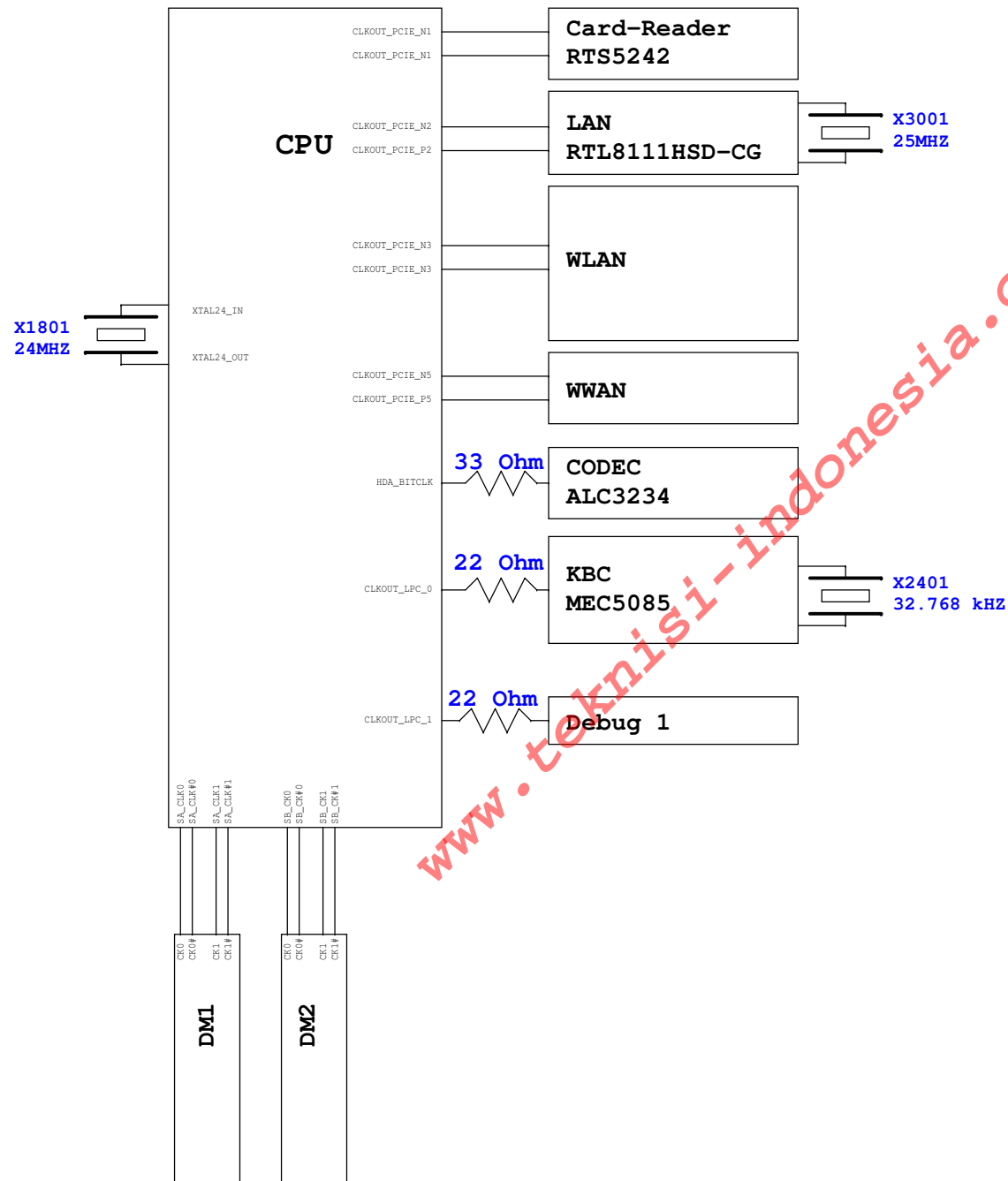
Thermal Block Diagram




Audio Block Diagram



Regulatory model:P47G
Regulatory Type:P47G002;Latitude 3350



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1	62	2015/5/12	EE	Vendor suggest increase ECE1117C ESD protection.	Add R6211	X01
2	47	2015/5/12	Power	This request by EMI . Because EMI test result is fail. So we msut add snubber to solve EMI issue .	1. Change PR4703 from 2.2R 0402 to 2.2R 0603 (64.2R205.55L) and stuff 2. Change PC4707 from 1500P to 1000P (78.10224.2FL) and stuff	X01
3	44	2015/5/13	Power	PL4401 after heat & vibration test will be broken. Change to a part with glue	Change PL4401 to 68.2R21C.10Q	X01
4	48/49	2015/5/13	Power	PL4801, PL4901 main source no share	PL4801, PL4901 change to 68.1R010.20I	X01
5	55	2015/5/25	EMC	To solve Broadwell ESD issue	Stuff U5502, U5503, U5504	X01
6	20/25	2015/6/2	EE	Add RTC circuit for factory request	Add RTC detect circuit : Q2502, R2506, R2021, R2022	X01
7	25	2015/7/1	EE	Change RTC circuit for RTC leakage	Mirror Q2502 vertically	X02
8	88	2015/7/1	EE	Fix TPM resume from DS3 will be lost issue	Change U8801 VSB form 3D3V_S5_PCH to 3D3V_S5	X02
9	24	2015/7/1	EE	Change board ID version	Change R2457 to 33K	X02
10	19/24	2015/7/9	EE	Fix alternative parts loop issue	Change both X1901 & X2401 to same 3 sources	X02
11	A11	2015/7/17	EE	Change to short pad	R402, R416, R417, R701, R704, R705, R706, R709, R1401, R1407, R1408, R1410 R1415, R1417, R1422, R1423, R1430, R1508, R1607, R1704, R1705, R1706, R1708 R1710, R1711, R1713, R1717, R1718, R1720, R1725, RN1801, RN1802, RN1803 RN1809, R1801, R1802, R1809, R1810, R1811, R1812, R1906, R1909, R2011, R2013 R2014, R2021, R2101, R2102, R2105, R2107, R2108, R2110, R2111, R2115, R2116 R2117, R2401, R2402, R2403, R2424, R2432, R2464, R2461, R2467, R2468, R2471 R2511, R2703, R2705, R2706, R2707, R2709, R2710, R2711, R2714, R2719, R2722 ER2701, ER2702, RN2701, R2738, R2740, R2741, R2742, R2745, R2911, EL2904 EL2903, R2912, R2902, R3006, R3001, R3201, R3206, R3217, R3202, R3204, R3207 R3209, R3210, R3211, R3213, R3212, R3301, R3401, R3402, R3403, R3405, R3407 R3408, R3409, R3412, R3601, R3610, R3603, R3604, R3637, R3654, R3656, R3619 R3611, R3655, R3625, R3657, PR4466, PR4434, PR4467, PR4430, PR4469 PR4501, PR4505, PR4521, PR4615, PR4625, PR4801, PR4903, R5217, R5222, R5221 R5227, R5406, R5407, R5601, R5602, R5603, R5604, R5820, R5830, R5808, R5806 R5828, R5829, R5924, R5927, R5928, R5901, R5906, R5905, R6115, R6103, R6201 R6202, R6203, R6207, R6701, R9620, R9807, R9906, R9903	X02
12	A11	2015/7/17	Power	Change to short pad	PR4406, PR4417, PR4430, PR4431, PR4434, PR4438, PR4466, PR4467, PR4469 PR4501, PR4505, PR4521, PR4615, PR4616, PR4617, PR4625, PR4801, PR4902 PR4903	X02
13	55	2015/7/17	EMC	Change for source reason	Change TR5501, TR5502, TR5503, TR5504 form 69.10118.001 to 068.24900.2001	X02
14	42	2015/7/20	Power	Change for source reason	Remove PD4402 2ND 083.10100.008R	X02
15	52	2015/7/21	ME	Change for source reason	Remove LCD1 main 20.F2089.030	X02
16	55	2015/7/21	ME	Change for source reason	Remove DP1 2nd 62.10105.431	X02
17	61	2015/7/21	ME	Change for source reason	Remove PWRBT1 2nd 62.40009.A81	X02
					<div> <div>Core Design</div> <div>  <div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div> </div> <div> <div>Title</div> <div>Change History-01</div> </div> <div> <div>Size</div> <div>Document Number</div> <div>Rev</div> <div>A00</div> </div> <div> <div>Date: Tuesday, August 18, 2015</div> <div>Sheet 107 of 110</div> </div> </div>	

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Dell

Wistron Corporation

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Title

Change History-02

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